

NAU83G60

DataSheet

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1 FEATURES

- Powerful Stereo Class-D Amplifier
Stereo 20W+20W Output Power @ 8Ω load, <1% THD+N, 24V V_{BAT}
Stereo 30W+30W Output Power @ 4Ω load, <10% THD+N, 24V V_{BAT}
Mono 30W continuous Output Power in PBTL (Parallel Bridge-Tied Load) mode @ 2Ω load, <10% THD+N, 24V V_{BAT}
- V_{BAT} : 8V ~ 24V
- On-Chip DSP Functions
2x 15-band PEQs
Up/Down Sampling Converter
- Programmable Serial Interfaces
High Speed I2C mode (up to 1Mbit/s)
TDM (I2S / PCM) Interface supports up to 8 channels & 192KHz sample rates
- Audio Clock Detection
- Device Protection
Short Current Protection (SCP)
Over Voltage Lock Out (OVLO)
Under Voltage Lock Out (UVLO)
Over Temperature Protection (OTP)
Clock Termination Protection (CTP)
- Battery Protection
Battery Limiter Control
- Speaker Protection
Current & Voltage Sensing
- Klippel Controlled Sound (KCS) Algorithm
Mechanical and Thermal Overload Protection
Linearization (Speaker Distortion Compensation)
Stabilization (Voice Coil Rest Position Stabilization)
Output Power and Voltage Limiter
Real-time Speaker Diagnostic Data
- Package: QFN 56 (7mm x 7mm)
- Applications
TV / Sound bar
Notebooks / Personal Computers / All in One PC
Wireless / Smart / Active Speakers

2 GENERAL DESCRIPTION

The NAU83G60 is a stereo 30W+30W smart amplifier with voltage and current sensing and integrated low latency Advanced Audio DSP running the KCS (Klippel Controlled Sound) speaker control algorithm. The hardware and software capabilities of NAU83G60 allow smaller speakers to be operated close to their physical limits. This expands their usable working range and enables safe operation with increased loudness, deeper bass, higher sound quality and maximum consistency. The adaptive nonlinear speaker control algorithm KCS provides reliable protection against thermal and mechanical overload, reduces harmonic and intermodulation distortion generated by speaker nonlinearities and cancels dynamic DC components in the voice coil displacement which allows the voice coil to be operated at its optimum rest position. It also compensates for speaker parameter variation due to production spread, aging and climate changes. These features provide significant advantages over the capabilities of conventional linear speaker protection algorithms.

The NAU83G60 integrates highly efficient Class D amplifiers with high performance 24-bit DACs for a stereo audio playback. In addition, it has two pairs of stereo 24-bit audio ADCs for current and voltage sensing at the speaker terminal with less gain variation over temperature and power supply for precision speaker control. The device can provide an accurate AEC (acoustic echo cancellation) reference signal to the host processor. This can improve the AEC barge-in performance significantly since the harmonic and intermodulation distortions can be synthesized and then compensated at the speaker output, producing a more linear, lower distortion system.

The NAU83G60 provides a flexible 15-band equalizer for precise control of the frequency spectrum. The Automatic Level Control (ALC) can control output level to the speaker, prevent speaker overload and optimize dynamic range. The integrated Under Voltage Lock-Out Protection (UVLOP) can monitor the battery voltage level and adjust the audio gain automatically to avoid possible output clipping issues. It also supports various device protection features such as OCP (Over Current Protection), OVLO (Over Voltage Lock Out), and OTP (Over Temperature Protection).

The NAU83G60 supports I2C control and TDM (I2S/PCM) audio interfaces. It operates with 3.3V digital supply voltages, while the battery supply voltage can operate from 8.0V to 24V. The operating temperature range is specified from -40°C to +85°C, and it is available in a QFN 56 (7mm x 7mm) package.

3 PART INFORMATION

3.1 Ordering Information

Product Category	Product Family	Optional Feature	Device Number	Package Type	Package Material	Option Mark	Temperature
NAU	83	G	60	Y	G		
NAU: Nuvoton Audio Product Line	83: Audio Amplifier Series	G: Green Speaker Amplifier Klippel Control Sound (KCS)	60: Total Output Power	Y: QFN-56 (7x7 mm ²)	G: Halogen-free RoHS-compliant TSCA-compliant	Blank: BTL P: PBTL	Blank: -40°C ~ +85°C

3.2 Pin Diagram

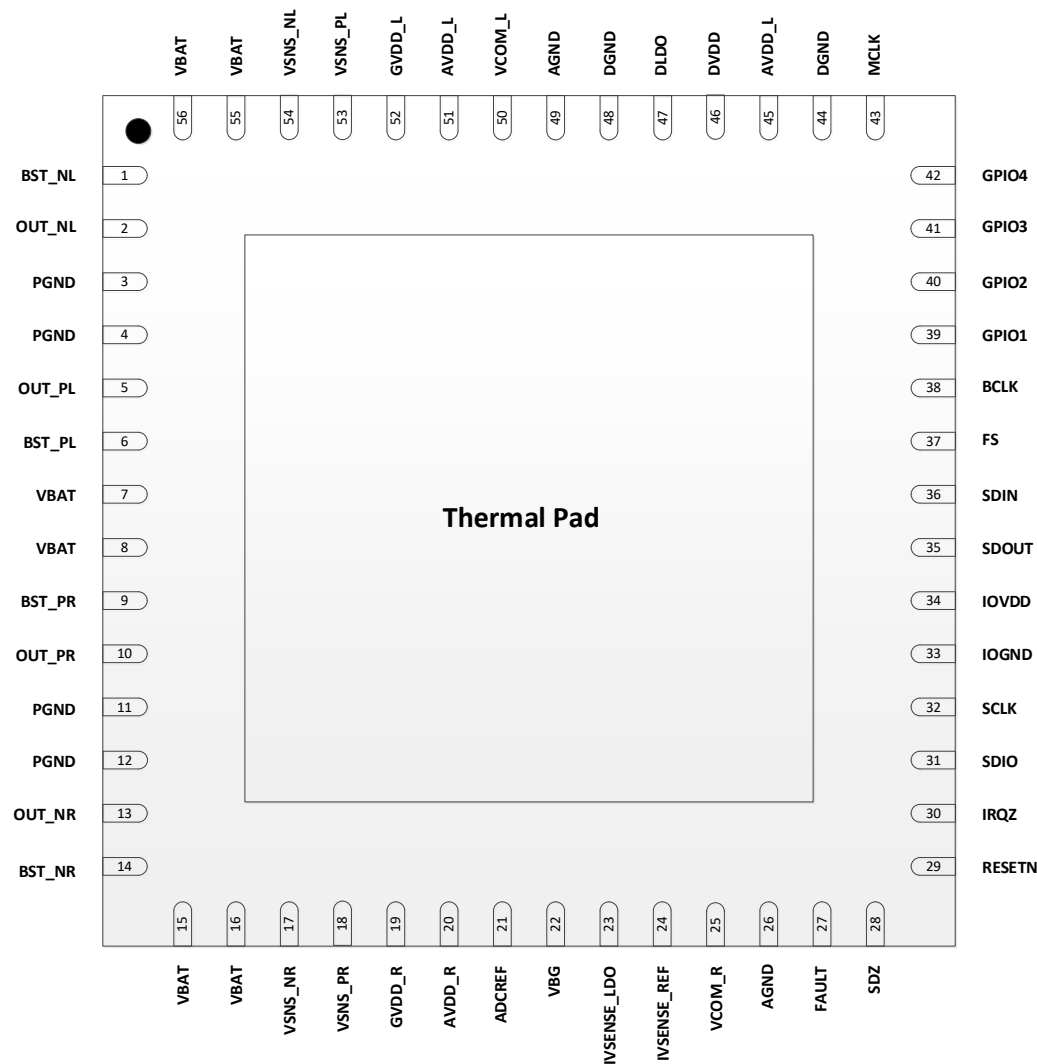


Figure 1 Pin Diagram of NAU83G60 (Top View)

3.3 Pin Description

Pin #	Name	Type	Functionality
0	EXP_PAD	P	Die Substrate Ground
1	BST_NL	I	Left Channel Bootstrap I/O, Negative High-Side FET
2	OUT_NL	O	Left Channel Negative Power Stage Output
3	PGND	P	Power Stage Ground
4	PGND	P	Power Stage Ground
5	OUT_PL	O	Left Channel Positive Power Stage Output
6	BST_PL	I	Left Channel Bootstrap I/O, Positive High-Side FET
7	VBAT	P	Class D Power Supply
8	VBAT	P	Class D Power Supply
9	BST_PR	I	Right Channel Bootstrap I/O, Positive High-Side FET
10	OUT_PR	O	Right Channel Positive Power Stage Output
11	PGND	P	Power Stage Ground
12	PGND	P	Power Stage Ground
13	OUT_NR	O	Right Channel Negative Power Stage Output
14	BST_NR	I	Right Channel Bootstrap I/O, Negative High-Side FET
15	VBAT	P	Class D Power Supply
16	VBAT	P	Class D Power Supply
17	VSNS_NR	I	Right Channel Voltage Sense Negative Input Connect To Class D Negative Output After Ferrite Bead
18	VSNS_PR	I	Right Channel Voltage Sense Positive Input. Connect to Class D Positive Output After Ferrite Bead Filter
19	GVDD_R	O	High Side FET Gate Drive Voltage Regulator Output. Decouple With Capacitor to GND
20	AVDD_R	P	Analog LDO Output. Decouple With Capacitor To GND
21	ADCREF	O	Reference Voltage Output Of SAR-ADC. Connect A Decoupling Capacitor to AGND
22	VBG	O	Reference Voltage Output of Bandgap. Connect A Decoupling Capacitor to AGND
23	IVSENSE_LDO	O	Voltage Regulator Output for IV _{Sense}
24	IVSENSE_REF	O	Reference Voltage Output of IV _{Sense} Connect A Decoupling Capacitor to AGND
25	VCOM_R	O	Common Mode Voltage. Decouple With Capacitor To AGND
26	AGND	P	Analog GND
27	FAULT	O	Fault Alert Pin
28	SDZ	I	Active Low Hardware Shutdown
29	RESETN	I	Chip Active Low Reset. Reset Whole Chip
30	IRQZ	O	Open Drain, Active Low Interrupt Pin
31	SDIO	I	I2C Data Pin. Pull Up to IOVDD With a Resistor
32	SCLK	I	I2C Clock Pin. Pull Up to IOVDD With a Resistor
33	IOGND	P	Digital IO GND
34	IOVDD	P	Digital IO Supply
35	SDOUT	O	TDM Serial Data Output in TDM Mode
36	SDIN	I	TDM Serial Data Input

Pin #	Name	Type	Functionality
37	FS	I	TDM Frame Sync
38	BCLK	I	TDM Serial Bit Clock
39	GPIO1	I/O	GPIO1 (I2C Address Selection)
40	GPIO2	I/O	GPIO2 (I2C Address Selection)
41	GPIO3	I/O	GPIO3
42	GPIO4	I/O	GPIO4
43	MCLK	I	External Clock Input Pin
44	DGND/FSOURCE	P I/O	Digital GND. Test Control Pin (Default: Connected To DGND)
45	AVDD_L_EFUSE	P	Power Supply of Efuse IP, Connect To AVDD_L
46	DVDD	P	Power Supply Input of Internal DREG Regulator. Decouple With Capacitor To DGND
47	DLDO	O	Digital Core Voltage Regulator Output. Decouple With Capacitor To DGND
48	DGND	P	Digital GND
49	AGND	P	Analog GND
50	VCOM_L	O	Common Mode Voltage. Decouple With Capacitor To AGND_DAC
51	AVDD_L	P	Analog Power Supply of Class D Analog Loop from Internal LDO. Decouple With a Capacitor To GND
52	GVDD_L	O	High Side FET Gate Drive Voltage Regulator Output. Decouple With Capacitor To GND
53	VSNS_PL	I	Left Channel Voltage Sense Positive Input.
54	VSEN_NL	I	Left Channel Voltage Sense Negative Input
55	VBAT	P	Class D Power Supply
56	VBAT	P	Class D Power Supply

Table 1 Pin Description Table

4 BLOCK DIAGRAM

Below is a block diagram for the NAU83G60 outlining the major internal blocks and signal flow.

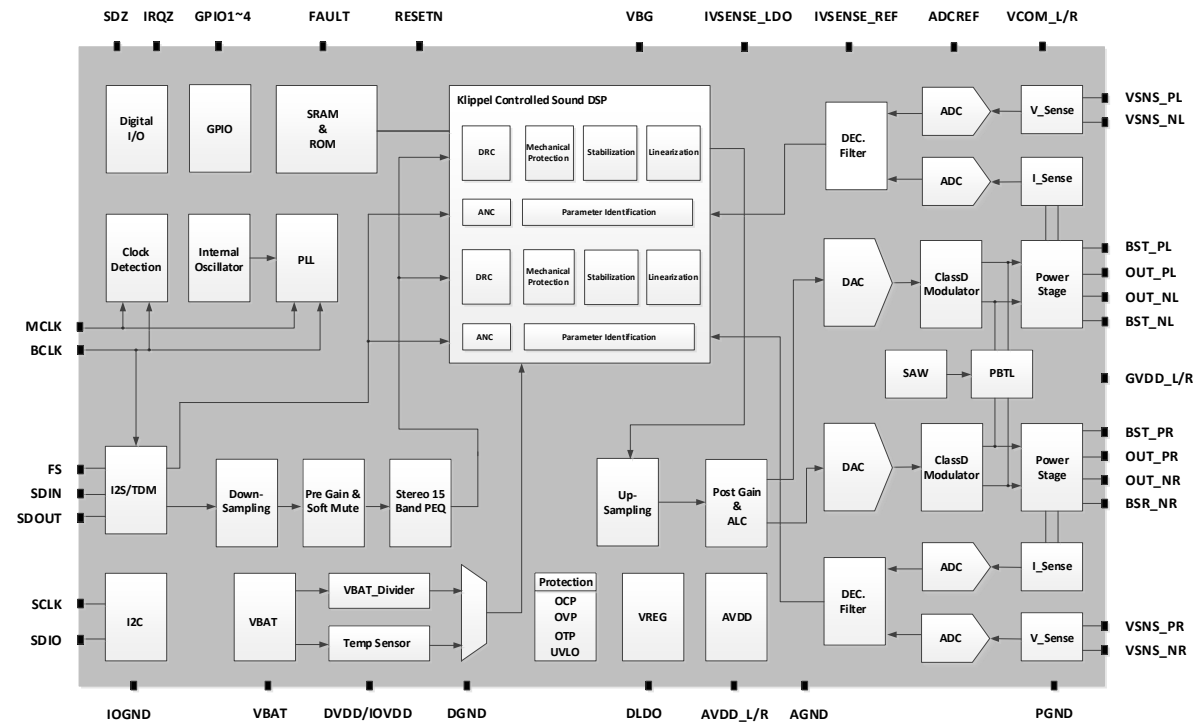


Figure 2 Block Diagram

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
IOVDD Digital I/O Supply Range	-0.3	3.8	V
DVDD Digital supply Range	-0.3	3.8	V
V _{BAT} Battery Supply Range	-0.3	26.0	V
Voltage Input I/O Range	DGND - 0.3	IOVDD + 0.3	V
Junction Temperature, T _J	-40	+150	°C
Storage Temperature	-65	+150	°C

Table 2 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

5.2 Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
V _{BAT} Analog Supply	V _{BAT}	8	12	24	V
Digital I/O Supply Range	IOVDD/DVDD	2.97	3.3	3.63	V
Ground	DGND		0		V
Operating Temperature		-40		+85	°C

Table 3 Operating Conditions

5.3 Thermal Information

THERMAL METRIC	Symbol	QFN56	Units
Junction-to-ambient thermal resistance	θ _{JA}	22.1	°C/W
Junction-to-case thermal resistance	θ _{JC}	8	
Junction-to-board thermal resistance	θ _{JB}	5.8	

Table 4 Operating Conditions

Default 4L PCB complies with JESD51 standard.

5.4 Digital I/O

Parameter	Symbol	Comments/Conditions	Min	Max	Units
Input LOW level	V_{IL}	IOVDD = 3.3V		0.3*IOVDD	V
Input HIGH level	V_{IH}	IOVDD = 3.3V	0.7*IOVDD		V
Output HIGH level	V_{OH}	$I_{Load} = 1\text{mA}$ IOVDD = 3.3V	0.95*IOVDD		V
Output LOW level	V_{OL}	$I_{Load} = 1\text{mA}$ IOVDD = 3.3V		0.05*IOVDD	V

Table 5 Digital I/O

5.5 Device Electrical Characteristics

Conditions: IOVDD = 3.3V; $V_{BAT} = 24\text{V}$. $R_L = 4\ \Omega$, $f = 1\text{KHz}$, 48KHz sample rate, MCLK=12.288MHz, MOD_GAIN=14dB, DAC_CUR_SET=1'b, HW2_VOL_L/R=0xBF66, Stereo BTL, unless otherwise specified.

Limits apply for $T_A = 25^\circ\text{C}$, Measured 15uH+0.68uF filter.

Symbol	Parameter	Comments/Conditions	Min	Typical	Max	Units
ISDH	Hardware Shutdown Supply Current (SDZ=Low)	IOVDD, Clocks Off		1	1.5	μA
		DVDD, Clocks Off		1	1.5	μA
		V _{BAT} = 12V, Clocks Off		25		μA
ISDS	RESET Supply Current	IOVDD, Clocks Off		175		μA
		DVDD, Clocks Off		200		μA
		V _{BAT} = 12V, Clocks Off		135		μA
ISB	Standby Mode Supply Current	IOVDD+DVDD, Clocks Off (PLL On), Analog Off		18		mA
		IOVDD+DVDD, Clocks Off (PLL Off), Analog Off		1.2		mA
		V _{BAT} = 12V, Analog Off		9		mA
IDD	Operating Mode Supply Current	IOVDD+DVDD, Idle Channel, DSP Off		80		mA
		V _{BAT} = 12V, Idle Channel, DSP Off		55		mA
		IOVDD+DVDD, Idle Channel, DSP/KCS On		88		mA
		V _{BAT} = 12V, Idle Channel, DSP/KCS On		78		mA
CLASS-D CHANNEL						
Po*	Output Power	RL = 8 Ω and Total Harmonic Distortion + Noise (THD+N) = 1%, BTL. V _{BAT} = 24V.		20		W

Symbol	Parameter	Comments/Conditions	Min	Typical	Max	Units
		MOD_GAIN=16dB, DAC_CUR_SET=0'b				
		R _L = 8 Ω and Total Harmonic Distortion + Noise (THD+N) = 10%, BTL, V _{BAT} = 24V, MOD_GAIN=16dB, DAC_CUR_SET=0'b		24		W
		R _L = 8 Ω and Total Harmonic Distortion + Noise (THD+N) = 1%, BTL, V _{BAT} = 24V, MOD_GAIN=14dB, DAC_CUR_SET=1'b		25		W
		R _L = 8 Ω and Total Harmonic Distortion + Noise (THD+N) = 10%, BTL, V _{BAT} = 24V, MOD_GAIN=14dB, DAC_CUR_SET=1'b		30		W
		R _L = 8 Ω and Total Harmonic Distortion + Noise (THD+N) = 1%, BTL, V _{BAT} = 12V		8		W
		R _L = 8 Ω and Total Harmonic Distortion + Noise (THD+N) = 10%, BTL, V _{BAT} = 12V		10		W
		R _L = 4 Ω and Total Harmonic Distortion + Noise (THD+N) = 1%, BTL, V _{BAT} = 12V		14.8		W
		R _L = 4 Ω and Total Harmonic Distortion + Noise (THD+N) < 10%, BTL, V _{BAT} = 12V		18		W
		R _L = 2 Ω and Total Harmonic Distortion + Noise (THD+N) < 10%, PBTL, V _{BAT} = 12V		35		W
THD+N	Total Harmonic Distortion + Noise	R _L = 8 Ω , f=1KHz, P _O = 0.25W, V _{BAT} = 12V		0.125		%
		R _L = 4 Ω , f=1KHz, P _O = 0.25W, V _{BAT} = 12V		0.125	0.15	
Eos	Output Noise	A-Weighted, 20Hz-20KHz, no DAC input signal, MOD_GAIN=14dB,		110		μV_{rms}

Symbol	Parameter	Comments/Conditions	Min	Typical	Max	Units
		DAC_CUR_SET=0'b ; V _{BAT} =12V				
		A-Weighted, 20Hz-20KHz, no DAC input signal, MOD_GAIN = 12dB, DAC_CUR_SET=0'b; V _{BAT} =12V		100		
PSRR	Power Supply Rejection Ratio	f _{ripple} = 1020Hz, V _{ripple} = 1V _{P-P}		70		dB
FRES	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, R _L = 4 Ω		±0.8		dB
V _{OS}	Output Offset Voltage	Idle Channel, V _{BAT} =12V		±2	±12	mV
K _{POP}	Pop and Click Noise	A-Weighted, Idle DAC Input, Clock Gating, Toggling Clocks On/Off		0.5		mV _{rms}
		A-Weighted, Idle DAC Input, Toggling Between - 120dBFS DAC In & 2048 Zero Samples		0.5		mV _{rms}
R _{DS(on)-P}	Driver P Side MOS- FET ON- resistance	V _{BAT} = 12V. Id=100 mA, Bond-wire Included		0.18		Ohm
R _{DS(on)-N}	Driver N Side MOS- FET ON- resistance	V _{BAT} = 12V. Id=100 mA, Bond-wire included		0.18		Ohm
F _{SW}	Switching Frequency	Average		432		kHz
P _{EFF}	Power Efficiency	V _{BAT} = 24V. R _L = 4 Ω + 33 μH, 10W+10W		81.5		%
		V _{BAT} = 12V. R _L = 4 Ω + 33 μH, 10W+10W		90		
T _{OTP}	Over Temperature Protection			145		°C
F _{SDAC} **	Calculated SPK Full Scale Output Level	MOD_GAIN=14dB, DAC_CUR_SET=1'b		23.3		Vp

Table 6 Device Electrical Characteristics

*: OTP could be triggered in high output power depending on thermal dissipation of PCBA

**.: The Full scale output level of KCS (Klippel Controlled Sound) speaker control algorithm is 18.5Vp

5.6 THD+N Plots

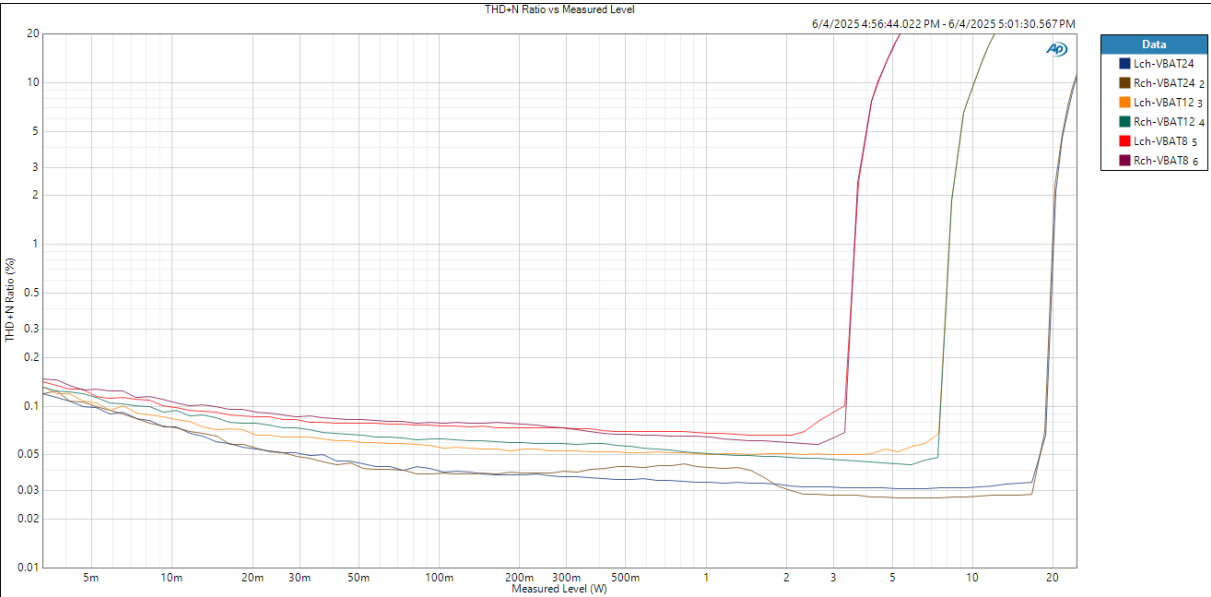


Figure 3 Output Power vs THD+N in Stereo BTL Output ($R_L = 8\ \Omega$, DAC_CUR_SET=0'b, MOD_GAIN=16dB)

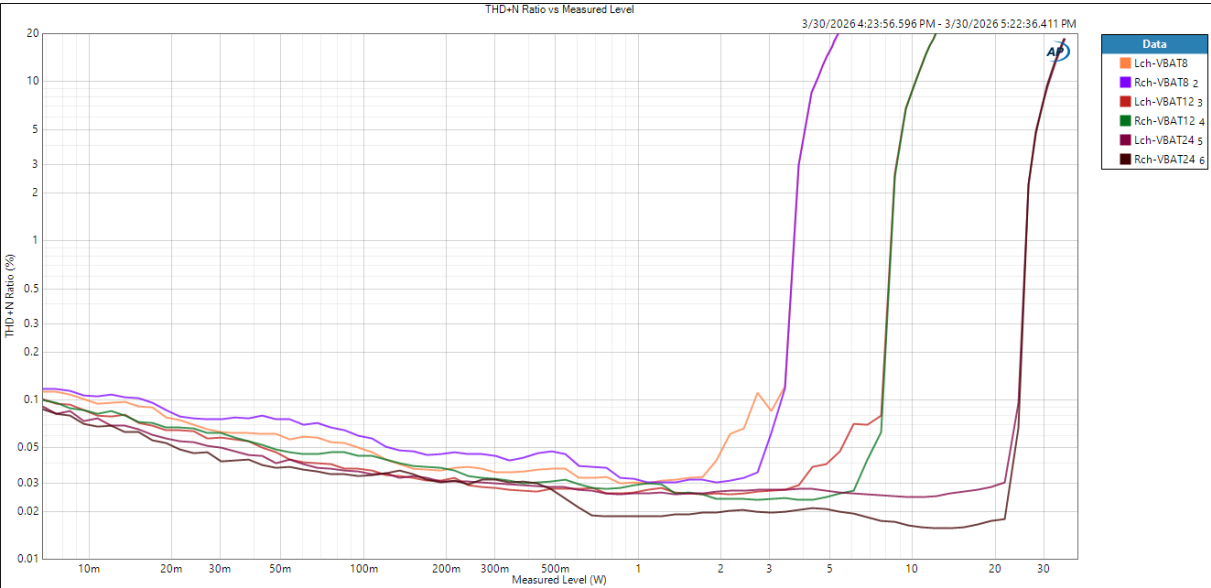


Figure 4 Output Power vs THD+N in Stereo BTL Output ($R_L = 8\ \Omega$, DAC_CUR_SET=1'b, MOD_GAIN=14dB)

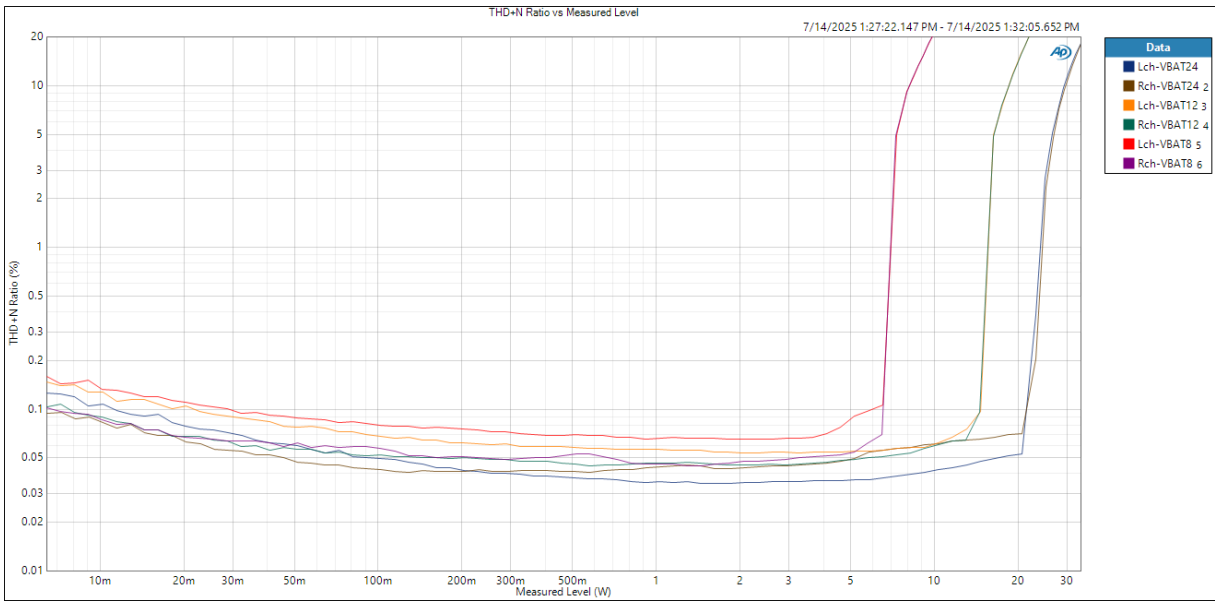


Figure 5 Output Power vs THD+N in Stereo BTL Output ($R_L = 4\text{ Ohm}$, $\text{DAC_CUR_SET}=0'b$, $\text{MOD_GAIN}=14\text{dB}$)

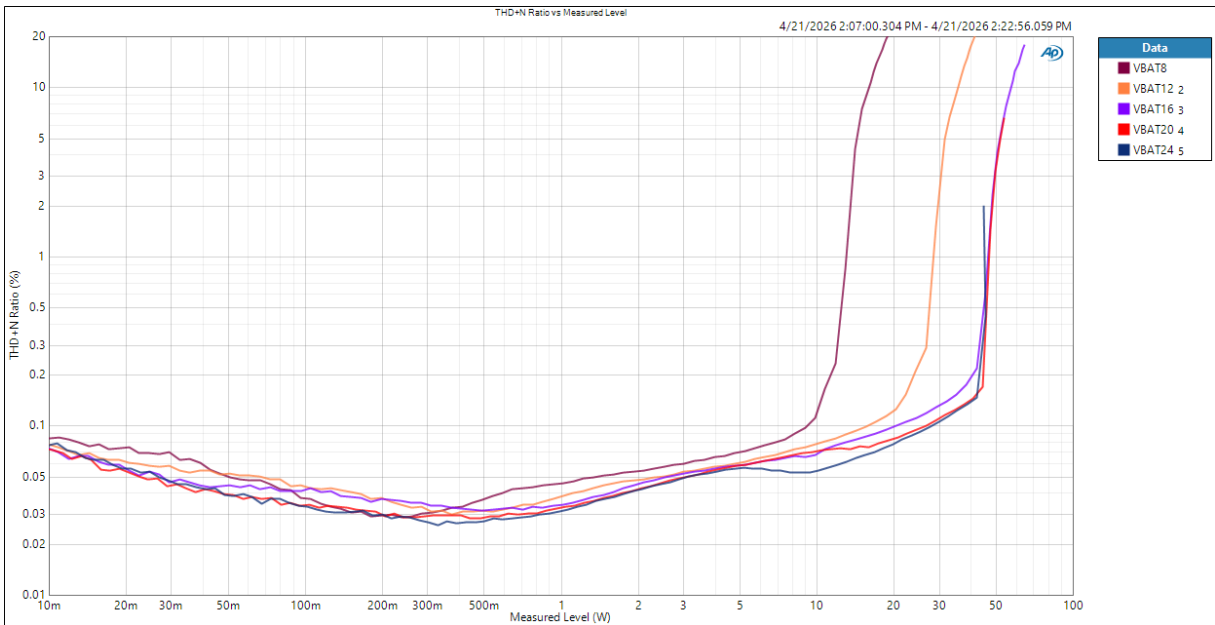


Figure 6 Output Power vs THD+N of PBTL ($R_L = 2\text{ Ohm}$, $\text{DAC_CUR_SET}=0'b$, $\text{MOD_GAIN}=14\text{dB}$)

5.7 Power Efficiency Plots

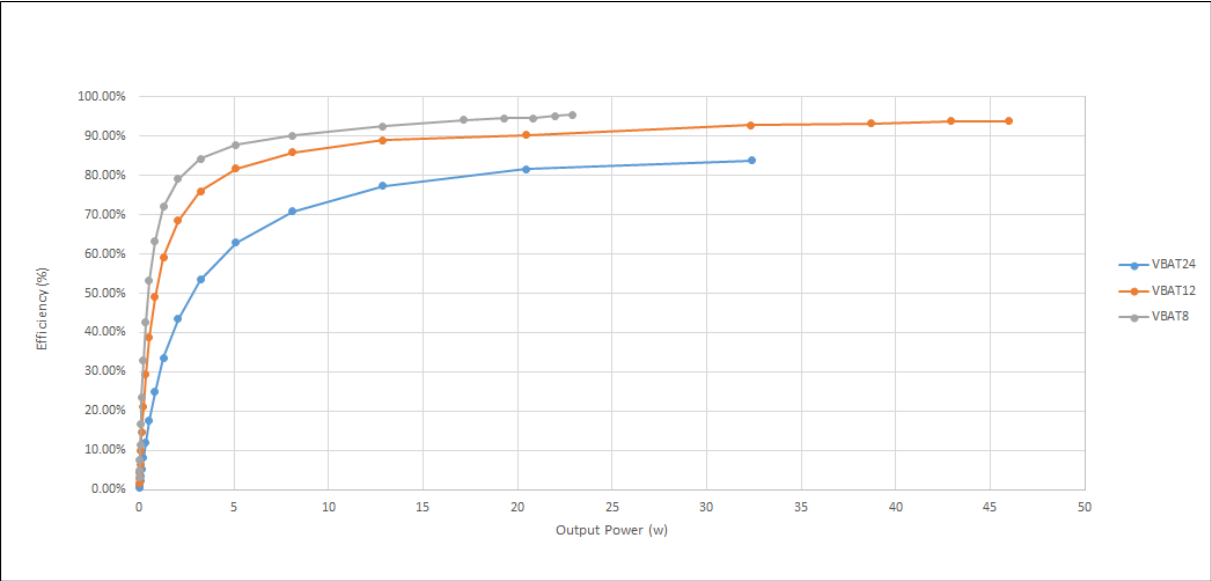


Figure 7 Output Power Efficiency - Stereo BTL (4 Ohm)

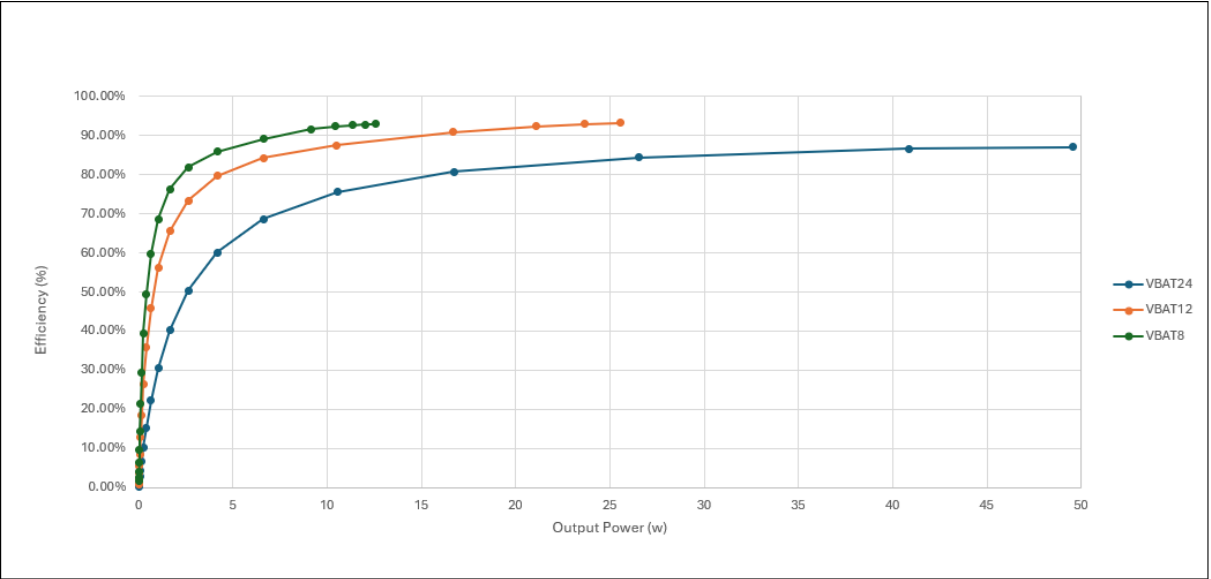
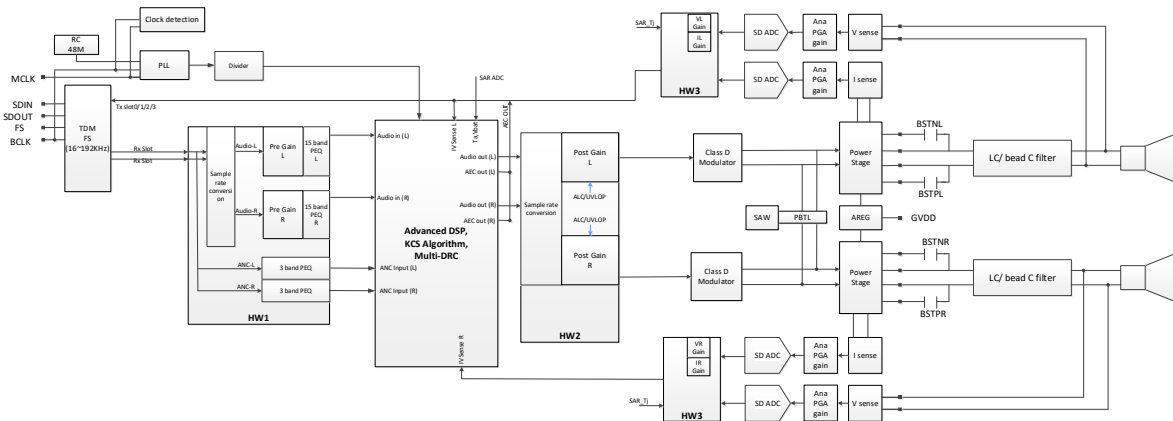


Figure 8 Output Power Efficiency - Stereo BTL (8 Ohm)

6 FUNCTIONAL DESCRIPTION

6.1 Audio Path

The NAU83G60 has two 24-bit Digital-to-Analog Converter (DAC) feeding Class-D modulators for a stereo audio playback and four high-quality Analog-to-Digital Converters (ADCs) for IV sensing per channel. These are high-performance, 24-bit sigma-delta converters. Advanced Audio DSP is embedded to run KCS (Klippel Controlled Sound) speaker control algorithm for enhancing speaker performance and protecting speaker. HW1, HW2, and HW3 enable a range of programmable signal conditioning and signal optimizing functions.



6.1.1 Audio PCM Path

NAU83G60 Audio PCM path supports 16KHz, 32KHz, 48KHz, 96KHz and 192KHz sample rates for audio playback from Host or record to Host. However, Advanced DSP only processes audio data in 48KHz sample rate. Therefore, except for the 48KHz sample rate, other sample rates need to be up/down sampled through HW1 before the Advanced DSP and down/up sampled through HW2 after the Advanced DSP.

44.1KHz, 88.2KHz and 176.4KHz sample rate can also be supported if clock source is multiple of 44.1KHz base instead of 48KHz base. The following description will only represent the 48KHz base.

In addition, NAU83G60 also supports TDM loopback path for debugging:

- Only 48KHz sample rates are supported if loop back from HW1 or Advanced DSP.
- Only 96KHz and 192KHz sample rates are supported if loop back from HW2. Please set **0x96[0].HW2_FS** to the same sample rate as input of TDM RX.

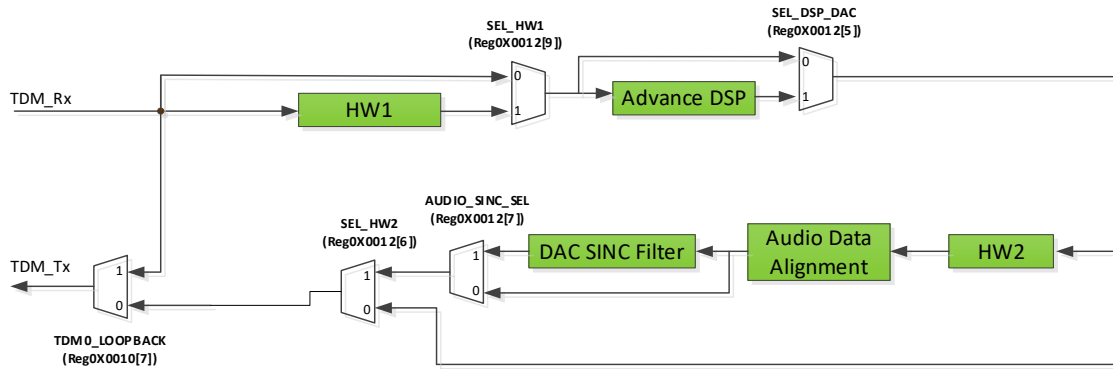


Figure 10 Audio PCM Look Back Path

Sample rate supported in Audio PCM loopback path:

Audio Loopback Path	Supported Sample rate
TDM direct loop back	16KHz, 32KHz, 48KHz, 96KHz and 192KHz
TDM -> HW1 -> TDM	48KHz
TDM -> HW1 -> Advanced DSP -> TDM	48KHz
TDM -> HW1 -> Advanced DSP -> HW2 -> TDM	96KHz and 192KHz
TDM -> HW1 -> HW2 -> TDM	96KHz and 192KHz

Table 7 Supported Sample Rates for Audio PCM Loopback Paths

Register Name	Address	Description / Range
REG_SRATE	0x40[12:10]	Audio Sampling rate (FS) setting 000 = 16K 001 = 32K 010 = 48K/44.1K 011 = 96K/88.2K 100 = 192K/176.4K

Register Name	Address	Description / Range
TDM_LOOPBACK	0x10[7]	TDM loopback 1 = Enabled 0 = Disabled
SEL_DSP_DAC	0x12[5]	0 = Bypass DSP path 1 = DSP path
SEL_HW2	0x12[6]	0 = Bypass HW2 path 1 = HW2 path
AUDIO_SINC_SEL	0x02[7]	0 = Bypass SINC filter 1 = SINC Filter path
SEL_HW1	0x12[9]	0 = Bypass HW1 1 = HW1 path
HW2_FS	0x96[0]	HW2 Output FS setting 0 = 96KHz 1 = 192KHz

Table 8 Audio PCM Loopback Path and Sample Rate Register Settings

6.1.2 AEC Audio Path

NAU83G60 provides Advanced DSP processed audio data as AEC reference through TDM-TX. NAU83G60 AEC path only supports 48KHz or 44.1KHz sample rates.

Set AEC audio slot length to **0X17[15].AEC_L_TX_SLEN** and **0X17[7].AEC_R_TX_SLEN 0X17[7]**. Assign AEC audio data to TDM TX slot by setting **0X17[13:8].AEC_L_TX_SLOT**, and **0X17[5:0].AEC_R_TX_SLOT**. Enable TDM TX for AEC audio data path by setting **0X17[14].AEC_L_TX_EN** and **0X17[6].AEC_R_TX_EN**. Please note that the unit of slot is in byte.

Register Name	Address	Description / Range
AEC_L_TX_EN	0x17[14]	TDM TX AEC L-CH enable 0 = Disabled 1 = Enabled
AEC_R_TX_EN	0x17[6]	TDM TX AEC R-CH enable 0 = Disabled 1 = Enabled
AEC_L_TX_SLEN	0x17[15]	TDM TX AEC L-CH slot length 0 = 2 slots (16-bit) 1 = 4 slots (32-bit)
AEC_R_TX_SLEN	0x17[7]	TDM TX AEC R-CH slot length 0 = 2 slots (16-bits) 1 = 4 slots (32-bits)
AEC_L_TX_SLOT	0x17[13:8]	TDM TX AEC L-CH slot
AEC_R_TX_SLOT	0x17[5:0]	TDM TX AEC R-CH slot

Table 9 AEC Path Registers

6.1.3 ANC Audio Path

NAU83G60 provides configurable low latency ANC path to Advanced DSP through TDM-RX. To reduce latency, NAU83G60 ANC path only supports 48KHz or 44.1KHz sample rates.

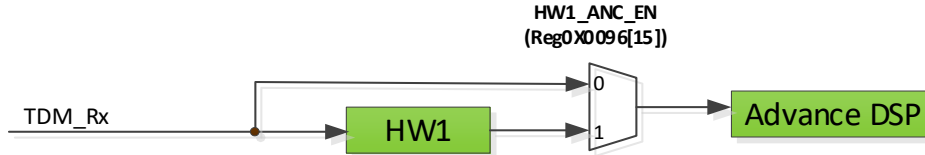


Figure 11 ANC Audio Path

Setting **0x10[15:12].RX_ANC_R** and **0x10[11:8].RX_ANC_L** for time slot of ANC. Set **0x96[1].ANC_LATENCY = 1'b1** can enable HW2 low latency if the path of ANC signal requires low latency. In addition, low latency function only supports 48KHz or 44.1KHz sample rate.

Register Name	Address	Description / Range
RX_ANC_L	0x10[11:8]	TDM RX ANC Left channel time slot
RX_ANC_R	0x10[15:12]	TDM RX ANC Right channel time slot
ANC_LATENCY	0x96[1]	HW2 ANC Low latency mode 0 = Normal 1 = Low latency
HW1_ANC_EN	0x96[15]	Enable 3 band PEQ for HW1 ANC path 0 = Disabled 1 = Enable 3 band PEQ

Table 10 ANC Path Registers

6.1.4 IV_{Sense} ADCs

The NAU83G60 has four high-quality Analog-to-Digital Converters (ADCs) for IV_{Sense} per channel to sense the voltage and current from speaker terminal for KCS algorithm through HW3. IV_{Sense} data can be transmitted to Host through TDM TX.

Register Name	Address	Description / Range
VSNS_L_SLEN	0x0D[7]	TDM TX V _{Sense} Left channel slot length 0 = 1 slot (8-bits) 1 = 2 slots (16-bits)
VSNS_R_SLEN	0x11[15]	TDM TX V _{Sense} Right channel slot length 0 = 1 slot (8-bits) 1 = 2 slots (16-bits)
VSNS_L_TX_EN	0x0D[6]	Transmission of V _{Sense} Left channel data 0 = Disabled 1 = Enabled
VSNS_R_TX_EN	0x11[14]	Transmission of V _{Sense} Right channel data 0 = Disabled 1 = Enabled

Register Name	Address	Description / Range
VSNS_L_SLOT	0x0D[5:0]	TDM TX Voltage sense Left channel time slot
VSNS_R_SLOT	0x11[13:8]	TDM TX Voltage sense Right channel time slot
ISNS_L_SLEN	0x0E[15]	TDM TX I _{sense} Left channel slot length 0 = 1 slot (8-bits) 1 = 2 slots (16-bits)
ISNS_R_SLEN	0x11[7]	TDM TX I _{sense} Right channel slot length 0 = 1 slot (8-bits) 1 = 2 slots (16-bits)
ISNS_L_TX_EN	0x0E[14]	Transmission of I _{sense} Left channel data 0 = Disabled 1 = Enabled
ISNS_R_TX_EN	0x11[6]	Transmission of I _{sense} Right channel data 0 = Disabled 1 = Enabled
ISNS_L_SLOT	0x0E[13:8]	TDM TX Current sense Left channel time slot
ISNS_R_SLOT	0x11[5:0]	TDM TX Current sense Right channel time slot

Table 11 IV_{sense} ADC Registers

6.2 KCS algorithm and Digital Signal Processor

The KCS (Klippel Controlled Sound) speaker control algorithm is implemented on the Advanced DSP (Digital Signal Processor). KCS uses voltage and current sensing signals for continuous identification of the instantaneous speaker parameters. KCS provides mechanical and thermal speaker protection while the adaptive and nonlinear control system cancels the DC voice coil displacement, reduces harmonic and intermodulation distortion generated by speaker nonlinearities. It also compensates for speaker parameter variation due to production spread, aging and climate changes. The audio sample rate of Advanced DSP is 48KHz. However, 44.1KHz sample rate can also be supported if clock source is multiple of 44.1KHz base.

For more information about the algorithm, please refer to <http://www.klippel.de/go/kcs>

6.3 HW Engines

In addition to Advanced DSP, there are three hardware engines, HW1, HW2, and HW3, for the Digital Signal Processing (DSP) subsystems that enable a range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and to maximize the audio dynamic range supported by the NAU83G60. These engines provide the up/down-sample rate conversion, PEQ, soft mute, gain adjustment, temperature compensation and low latency ANC path.

HW Engine 1 (HW1) supports up/down-sample rate converter, soft mute/unmute to avoid pop noise and gain adjustment (Pre Gain). Sample rate converter will convert 16KHz/32KHz sample rate to 48KHz sample rate or 96/192KHz sample rate to 48KHz sample rate. Please note that below description only mentioned for 48KHz base sample rate, however, 44.1Kz sample rate can be calculated proportionally.

HW Engine 2 (HW2) supports up-sample rate converter, Post Gain control for ALC/UVLOP. Up-sample rate converter to convert 48KHz sample rate to 96/192KHz sample rate (44.1Kz sample rate can be

calculated proportionally). UVLOP function will monitor the voltage of battery (V_{BAT}) to adjust the digital signal level to prevent clipping if the voltage of battery drops precipitously. Please note that below description only mentioned for 48KHz base sample rate, however, 44.1Kz sample rate can be calculated proportionally.

HW Engine 3 (HW3) supports the digital gain adjustment for the voltage/current sense (IV_{Sense}) data from Class-D amplifier. The Voltage and current sense data will be corrected with temperature compensation to obtain optimal performance.

6.3.1 Hardware Engine 1 (HW1)

NAU83G60 Audio PCM path supports 16KHz, 32KHz, 48KHz, 96KHz and 192KHz sample rates for audio playback from Host or record to Host. However, Advanced DSP only processes audio data in 48KHz sample rate. Therefore, except for the 48KHz sample rate, other sample rates need to be up/down sampled through HW1 before the Advanced DSP and down/up sampled through HW2 after the Advanced DSP.

HW1 is placed between TDM input and Advanced DSP. It plays the key role as sample rate converter, digital gain adjustment with soft mute and PEQ.

HW1 also converts different input sample rate to be compatible with KCS algorithm. If the input sample rate is 16KHz or 32KHz, it will up-sample to 48KHz. If the input sample rate is 96KHz or 192KHz, it will down-sample to 48KHz. If the sample rate is 48Hz, the up/down sample is not active.

After up/down sample, the signal level can be adjusted by Input volume gain registers **0x9A[15:0].HW1_VOL_L** and **0x9B[15:0].HW1_VOL_R**.

The soft mute/unmute can avoid pop noise during mute/unmute **0x9C[8].HW1_CH_MUTE**. The attack/recover time can be adjusted by the register **0x9C[10:9].HW1_VSR** for preferred characteristics. When the soft unmute/unmute is active, the gain will be changed only when signal zero cross happens.

Register Name	Address	Description / Range
HW1_VOL_L	0x9A[15:0]	HW1 volume gain Left channel
HW1_VOL_R	0x9B[15:0]	HW1 volume gain Right channel
HW1_CH_MUTE	0x9C[8]	HW1 soft mute control 0 = Un-mute 1 = Mute
HW1_VSR	0x9C[10:9]	HW1 gain adjust slew rate 00 = 0.5 dB 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB

Table 12 HW1 Volume Registers

6.3.1.1 PEQ (Parametric Equalizer)

HW1 also includes a 15-band high precision PEQ (Parametric Equalizer): BIQ0~BIQ14 to provide flexible frequency response. But when the ANC is enabled by setting **0x96[15].HW1_ANC_EN** =1'b1, bands 12/13/14 of PEQ will be transferred as 3rd Order IIR Filter for ANC path.

The register **0x9D[15:12].PEQ_BAND** controls the numbers of PEQ to be activated, and start from BIQ0. The coefficients of each band are placed in the register table as defined below:

PEQ	Left Channel Address	Right Channel Address
BIQ0	0x0100 ~ 0x0109	0x0200 ~ 0x0209
BIQ1	0x010c ~ 0x0115	0x020c ~ 0x0215
BIQ2	0x0118 ~ 0x0121	0x0218 ~ 0x0221
BIQ3	0x0124 ~ 0x012d	0x0224 ~ 0x022d
BIQ4	0x0130 ~ 0x0139	0x0230 ~ 0x0239
BIQ5	0x013c ~ 0x0145	0x023c ~ 0x0245
BIQ6	0x0148 ~ 0x0151	0x0248 ~ 0x0251
BIQ7	0x0154 ~ 0x015d	0x0254 ~ 0x025d
BIQ8	0x0160 ~ 0x0169	0x0260 ~ 0x0269
BIQ9	0x016c ~ 0x0175	0x026c ~ 0x0275
BIQ10	0x0178 ~ 0x0181	0x0278 ~ 0x0281
BIQ11	0x0184 ~ 0x018d	0x0284 ~ 0x028d
BIQ12	0x0190 ~ 0x0199	0x0290 ~ 0x0299
BIQ13	0x019c ~ 0x01a5	0x029c ~ 0x02a5
BIQ14	0x01a8 ~ 0x01b1	0x02a8 ~ 0x02b1

Table 13 PEQ Band Register Addresses

The sequence to write coefficients of each band of PEQ to HW1 engine is:

1. Set **0x9D[0].PEQ_STALL** =1'b1
2. Set **0x9D[1].HW1_MEM_CLEAR** =1'b1
3. Set **0x9D[1].HW1_MEM_CLEAR** =1'b0
4. Set **0x9D[2].HW1_MEM_WR** =1'b1
5. Write coefficient (L-ch: REG0X0100~REG0X01B1, R-ch:REG0X0200~REG0X02B1)
6. Set **0x9D[2].HW1_MEM_WR** =1'b0
7. Set **0x9D[0].PEQ_STALL** =1'b0

User must initialize PEQ parameters after power on. Please use NAU83G60 GUI to generate the parameters of PEQ.

Register Name	Address	Description / Range
PEQ_BAND	0x9D[15:12]	The numbers of PEQ to be activated
PEQ_STALL	0x9D[0]	0 = Normal run 1 = Stall PEQ
HW1_MEM_CLEAR	0x9D[1]	0 = Normal run 1 = Clear DRAM
HW1_MEM_WR	0x9D[2]	0 = Normal run 1 = Write coefficients
HW1_ANC_EN	0x96[15]	HW1 ANC Function Enable 0 = Disabled (Downsample / Upsample) 1 = Enabled (Downsample / Upsample + 3 BIQ)

Table 14 PEQ Initialization Register Settings

6.3.2 Hardware Engine 2 (HW2)

HW2 is placed between Advanced DSP and 24-bit DAC. It plays the role of sample rate converter, digital gain adjustment with soft mute and digital post gain which is controlled by the ALC/UVLOP function. It receives the data from the output buffer of Advanced DSP which is processed by KCS which combines ANC and audio data for processing. HW2 can also provide low latency ANC path when required. The output of HW2 is 24-bit DACs.

If the TDM input samples are 96KHz or 192KHz, HW2 can be used to up sample 48KHz Advanced DSP processed audio data to the same sample rate as the input by setting **0x96[0].HW2_FS** before outputting it by TDM TX.

Register Name	Address	Description / Range
HW2_STALL	0x90[13]	0 = Normal run 1 = Stall HW2
HW2_EN	0x96[5]	Hw2 Function Enable 0 = Disabled 1 = Enabled
HW2_DROOP_SEL	0x96[3]	Droop Mode Select 0 = Small 1 = Large
HW2_DROOP_EN	0x96[2]	Droop Function Enable 0 = Disabled 1 = Enabled
ANC_LATENCY	0x96[1]	HW2 Low Latency Mode 0 = Normal 1 = Low Latency (For ANC Path)
HW2_FS	0x96[0]	HW2 Output FS setting 0 = 96KHz

Register Name	Address	Description / Range
		1 = 192KHz
Hw2_Vol_L	0x97[15:0]	Hw2 Volume Gain Left Channel
Hw2_Vol_R	0x98[15:0]	Hw2 Volume Gain Left Channel
HW2_CH_MUTE	0x99[8]	HW2 Soft Mute Control 0 = Un-mute 1 = Mute
HW2_VSR	0x99[10:9]	HW2 Gain Adjust Slew Rate 00 = 0.5 dB 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB

Table 15 HW2 Function Register Settings

6.3.3 Hardware Engine 3 (HW3)

HW3 is placed between voltage sense ADC / current sense ADC and Advanced DSP. It receives the processed V_{Sense}/I_{Sense} data and adjust the digital level by VL-Gain/IL-Gain. Since the performance of I_{Sense} is influenced by the temperature. The HW3 will reference the T_j (junction temperature) from SARADC to compensate the I_{Sense} data and output to Advanced DSP. Both I_{Sense} and V_{Sense} ADC data can be output to Host through TDM-TX.

Register Name	Address	Description / Range
HW3_STALL	0x86[13]	0 = Normal Run 1 = Stall HW3
HW3_EN	0x8C[3]	HW3 Function Enable 0 = Disabled 1 = Enabled
HW3_DROOP_SEL	0x8C[2]	Droop Mode Select 0 = Large 1 = Small
HW3_FS	0x8C[0]	HW3 Input Data Sample Rate 0 = 96KHz (Downsample 96K to 48K) 1 = 192KHz (Downsample 192K to 48K)
HW3_VOL_VL	0x8A[15:0]	V_{Sense} Volume Gain Left Channel
HW3_VOL_VR	0x8B[15:0]	V_{Sense} Volume Gain Right Channel
HW3_VOL_IL	0x8D[15:0]	I_{Sense} Volume Gain Left Channel
HW3_VOL_IR	0x8E[15:0]	I_{Sense} Volume Gain Right Channel
HW3_CH_MUTE	0x8F[8]	HW3 Soft Mute Control 0 = Un-mute 1 = Mute

Register Name	Address	Description / Range
HW3_VSR	0x8F[10:9]	HW3 Gain Adjust Slew Rate 00 = 0.5 dB 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB

Table 16 HW3 Function Register Settings

6.4 Soft Mute

The HW1 implements a programmable digital gain with soft mute/unmute function. It can ramp down the audio digital volume to zero. Setting **0x9C[8].HW1_CH_MUTE** can mute/unmute the audio signal input into Advanced DSP by Hardware Engine 1. **0x9C[10:9].HW1_VSR** sets the slew rate of HW1 soft mute/unmute.

The HW2 implements a programmable digital gain with soft mute/unmute function. It can ramp down the audio digital volume to zero. Setting **0x99[8].HW2_CH_MUTE** can mute/unmute the audio signal output from Advanced DSP by Hardware Engine 2. **0x99[10:9].HW2_VSR** sets the slew rate of HW2 soft mute/unmute.

HW3 also implement a programmable digital gain with soft mute function, setting **0x8F[8].HW3_CH_MUTE** can mute/unmute the $I_{V_{sense}}$ signal input into Advanced DSP by Hardware Engine 3. **0x8F[10:9].HW3_VSR** sets the slew rate of HW3 soft mute/unmute.

Register Name	Address	Description / Range
HW1_CH_MUTE	0x9C[8]	HW1 Soft Mute Control 0 = Un-mute 1 = Mute
HW1_VSR	0x9C[10:9]	HW1 Gain Adjust Slew Rate 00 = 0.5 dB 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB
HW2_CH_MUTE	0x99[8]	HW2 Soft Mute Control 0 = Un-mute 1 = Mute
HW2_VSR	0x99[10:9]	HW2 Gain Adjust Slew Rate 00 = 0.5 dB 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB
HW3_CH_MUTE	0x8F[8]	HW3 Soft Mute Control 0 = Un-mute

Register Name	Address	Description / Range
		1 = Mute
HW3_VSR	0x8F[10:9]	HW3 Gain Adjust Slew Rate 00 = 0.5 dB 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB

Table 17 Soft Mute Control Register Setting

6.5 Power Supply

The NAU83G60 only needs two external power source to operate. The V_{BAT} is designed to connect with the external power supply or battery cells which the voltage range is 8V~24V as the analog domain power source. The IOVDD and DVDD is designed to connect with an external supply or PMIC of which the voltage range is 3.3V as the digital domain power source.

There are four internal LDO regulated supplies (DLDO/ALDO for AVDD)/GLDO for GVDD/IVSENSE_LDO), to provide the excellent PSRR performance with low noise and low quiescent current.

Set RESETN pin to LOW can reset whole chip.

6.5.1 Power-On/Off Timing

Please refer to Figure 12 for the Power-on/off procedure.

- V_{BAT} power on and reaches > 5V before DVDD/IOVDD power on; V_{BAT} powers off after DVDD/IOVDD.
- SDZ can be connected together with DVDD/IOVDD. Alternatively, when power on, SDZ can also be set HIGH after DVDD/IOVDD; when power off, SDZ can be set LOW before DVDD/IOVDD.
- When power on, RESETN should be held LOW for > 10ms after SDZ set HIGH. When power off, RESETN should be set LOW before SDZ set LOW.
- When power on, wait at least 1ms after MCLK/BCLK ready before driver Initialization by I2C interface.

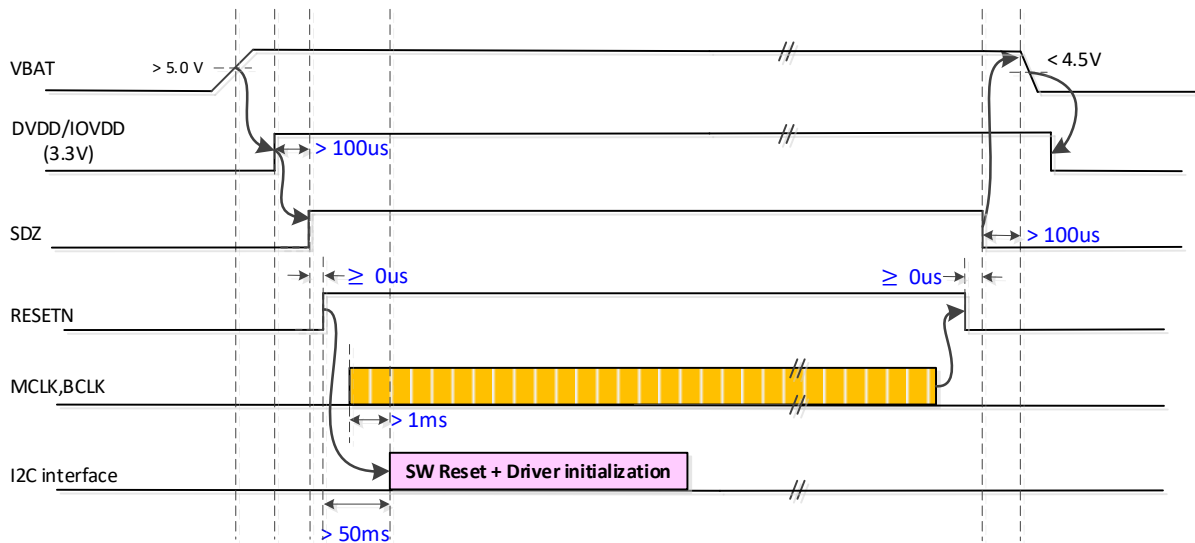


Figure 12 Power ON/OFF Timing

For reliable operation, it is recommended to write to register **0x00.RESET_N1** during Driver initialization upon power-up. This will reset all registers to the known default state.

6.6 Hardware Reset and Software Reset

The NAU83G60 and all of its control registers can be reset to initial default power-up conditions by writing 0x5A5A then 0xA5A5 to **0x00.RESET_N1**. Besides, state-machine and analogue design are reset to default. This is typically done during hardware reset.

The state machine of NAU83G60 can be reset to initialized power-up conditions by writing 0x5A5A then 0xA5A5 to **0x01.RESET_N_SOFT_PRE**, but all registers values will be unaffected. This is typically done during operation to quickly force NAU83G60 to a known initialized startup state.

Register Name	Address	Description / Range
RESET_N1 (WO)	0x00[15:0]	Write 0x5A5A -> 0xA5A5 to this register to reset all the registers. 0x5A5A = Enable the internal SW reset. 0xA5A5 = Release the internal SW reset.
RESET_N_SOFT_PRE	0x01[15:0]	Write 0x5A5A -> 0xA5A5 to this register to reset all internal stated machines without resetting the registers. 0x5A5A = Enable the internal SW reset. 0xA5A5 = Release the internal SW reset.

Table 18 Register Setting for Hardware Reset and Software Reset

6.7 Voltage Reference

The NAU83G60 includes four pins for voltage references: VCOM_L, VCOM_R, ADCREF and IVSENSE_REF. The VCOM is the mid-supply reference circuit of each channel that produces voltage close to AVDD/2 that is decoupled to AGND through the VCOM_L pin and VCOM_R pin by means of an external bypass capacitor. Because VCOM are used as a reference voltage for the majority of the NAU83G60, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 μ F is used.

The ADCREF pin and IVSENSE_REF pin are used as the reference voltage for the SARADC and IV sense ADC, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 μ F is used.

APPLICATION NOTES:

- Larger capacitances can be used but increase the rise time of VREF and delay the line output signal.
- Due to the high impedance of the VREF pin, it is important to use a low-leakage capacitor.

6.8 Clocks

The digital/analog system clock can be generated from MCLK/PLLOUT/BCLK/HIRC48M. MCLK is suggested to provide externally from Host to meet Table 23. However, it is noted that some Host can't provide the MCLK output but the NAU83G60 can still generate the system clock from the BCLK by fraction-N PLL to provide wide input/output clock range. The PLL input frequency is suggested to be within 1MHz to 10MHz while output frequency is suggested to be configured to 122.88MHz (48KHz base sample rate) or 112.896MHz (44.1KHz base sample rate) for audio system clock and operation of Advanced DSP and Hardware engine. The internal HIRC48M is another system clock source that can be utilized if host clocking fails. This allows protection of output driver.

Please note that in this document, some descriptions of clock setting only mentioned for 48KHz base sample rate, however, the clock setting for 44.1Kz sample rate can be calculated proportionally.

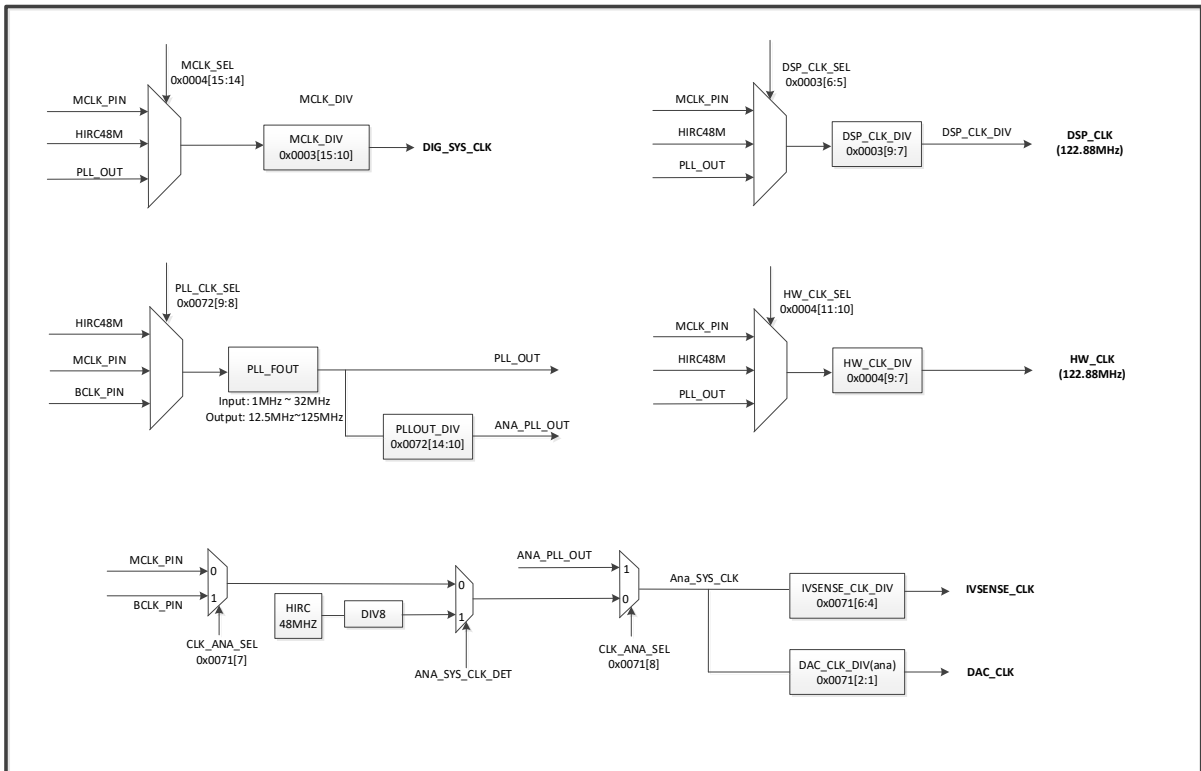


Figure 13 NAU83G60 Clock Tree (48KHz Sample Rate Base)

Register Name	Address	Description / Range
MCLK_DIV	0x03[15:10]	MCLK Divider = MCLK_DIV + 1
DSP_CLK_DIV	0x03[9:7]	DSP_CLK divider = DSP_CLK_DIV + 1
DSP_CLK_SEL	0x03[6:5]	00 = MCLK 01 = RC48M 10 = PLL 11 = Reserved

Table 19 DSP Clock Source Registers

Register Name	Address	Description / Range
MCLK_SEL	0x04[15:14]	00 = MCLK 01 = RC48M 10 = PLL 11 = Reserved
HW_CLK_SEL	0x04[11:10]	00 = MCLK 01 = RC48M 10 = PLL 11 = Reserved
HW_CLK_DIV	0x04[9:7]	HW_CLK divider = HW_CLK_DIV + 1

Table 20 HW Clock Source Selection Registers

Register Name	Address	Description / Range
IVSNS_CLK_INV_SEL	0x71[10]	0 = Normal 1 = Inverter
PD_ANA_CLK	0x71[9]	Power Down of Analog Clock for DAC And IV _{Sense} ADC 0 = Enable clock 1 = Power down clock
CLK_ANA_SEL	0x71[8:7]	Select of Analog Clock Source 00 = MCLK 01 = BCLK Others = ANA_PLL
IVSNS_CLK_DIV	0x71[6:4]	Divider Setting of IV _{Sense} ADC Clock 000 = Div 1 001 = Div 2 010 = Div 4 011 = Div 5 100 = Div 8 101 = Div 10
DAC_CLK_DIV	0x71[2:1]	Divider Setting of DAC Clock Source 00 = Div 1 01 = Div 2 10 = Div 4 11 = Div 8

Table 21 Analog Clock Source Selection Divider Registers

Register Name	Address	Description / Range
PLL_DIV_RESET	0x72[15]	Reset of PLL Dividers 0 = Reset 1 = Not reset
PLLOUT_DIV	0x72[14:10]	PLL Output Divider Setting for Analog Clock. This Register Is Used When Analog DAC/ADC Use the PLL Divided Clock. Output Divider Number=PLLOUT_DIV+1
PLL_CLK_SEL	0x72[9:8]	Select The Reference Clock Input of the PLL. 00 = MCLK 01 = BCLK 10 = Reserved 11 = RC48M
PD_PLL	0x72[7]	Power of PLL 0 = Enabled 1 = Disabled (default)
PLL_RSEL	0x73[14:13]	PLL output divider setting The divider set the PLL VCD output setting 00 = FVCO div 1 01 = FVCO div 2 10 = FVCO div 3 11 = FVCO div 4
PLL_MSEL	0x73[12:8]	PLL input divider setting Input divider number=MSEL+1 For example, 00000 = Div 1 (bypass) 11111 = Div32
PLL_NSEL	0x73[7:0]	PLL feedback divider setting. Feedback divider number = (NSEL.XSEL) + 1
PLL_XSEL	0x74[11:0]	

Table 22 PLL Configuration Registers

The Frequency of PLL_OUT can be configured according PLL_IN frequency and the register setting of **0x73[7:0].PLL_NSEL**, **0x74[11:0].PLL_XSEL**, **0x73[12:8].PLL_MSEL** and **0x73[14:13].PLL_RSEL** according to formula below:

$$PLL_OUT = PLL_IN * ((PLL_NSEL + 1).PLL_XSEL)/((PLL_MSEL + 1) * (PLL_RSEL + 1))$$

6.8.1 MCLK/BCLK Clock Divider

The NAU83G60 includes several dividers: MCLK_DIV, HW_CLK_DIV, DSP_CLK_DIV, DAC_CLK_DIV and IVSENSE_CLK_DIV to provide suitable frequency for internal clock usage. Depending on the sample rate setting and MCLK/FS and BCLK/FS ratio, the user needs to configure these divider registers appropriately. Please see Figure 13.

DIG_SYS_CLK needs to be configured to the same frequency as the **0x40[9:7].MCLK_RATE** setting. Typical frequency is 12.288MHz. The PLL_OUT is suggested to set to 122.88MHz if used. In addition, DIG_SYS_CLK frequency needs to be higher than 2 x BCLK frequency.

Audio DAC and IV_{Sense} ADC clock setting need to be configured according to Table 23 depending on MCLK frequency or PLL clock generated from BCLK.

MCLK (MHz)	DSP rate (KHz)	0x96[0].HW2_FS	DAC SINC, SDM output (MHz)	DAC_CLK (MHz)	0x5D[5:4].DAC_SINC_OS	IVSENSE_CLK (MHz)	0x5D[0:1].IVSENSE_SINC_OS
11.2896	44.1	1'b1	5.6448	5.6448	2'b01	5.6448	2'b01
12.288	48	1'b1	6.144	6.144	2'b01	6.144	2'b01
22.5792	44.1	1'b1	5.6448	5.6448	2'b01	5.6448	2'b01
24.576	48	1'b1	6.144	6.144	2'b01	6.144	2'b01
From PLL = 122.88	48	1'b1	6.144	6.144	2'b01	6.144	2'b01

Table 23 Audio DAC and IV_{Sense} ADC Clock Settings

NAU83G60 supports different sample rates and BCLK listed in Table 36.

6.8.2 DSP clock & Hardware Engine clock

The clock for the DSP and the Hardware engines are generated from external MCLK, internal RC clock or embedded PLL block. The frequency of this clock is 122.88MHz. Please see Figure 13.

6.9 Audio Clock Detection

The NAU83G60 includes an Audio Clock Detection circuit that can be used to enable and disable the audio paths based on an initialized audio path setting. Enable the audio path through the I2C Interface; but, the actual power up/down can be gated by the Audio Clock Detection circuit. Audio Clock Detection circuit sense the external clock MCLK, FS and BCLK. It also computes the ratio of MCLK/FS and BCLK/FS to configure correct clock setting.

The Audio Clock Detection works when BCLK is 32bits or more than 32bits per Fs format. For external FS and MCLK, the registers **0x40[12:10].REG_SRATE** and **0x40[9:7].MCLK_RATE** need to be set to correct values.

When **0x41[1].EN_AMCLKDET**= 1'b1 and **0x41[3].EN_ABCLKDET** =1'b1, the NAU83G60 will detect abnormal system operation, and the Audio Clock Detection will automatically switch the system clock source from MCLK to internal HIRC48M clock by **ANA_SYS_CLK_DET** asserted if external MCLK is lost.

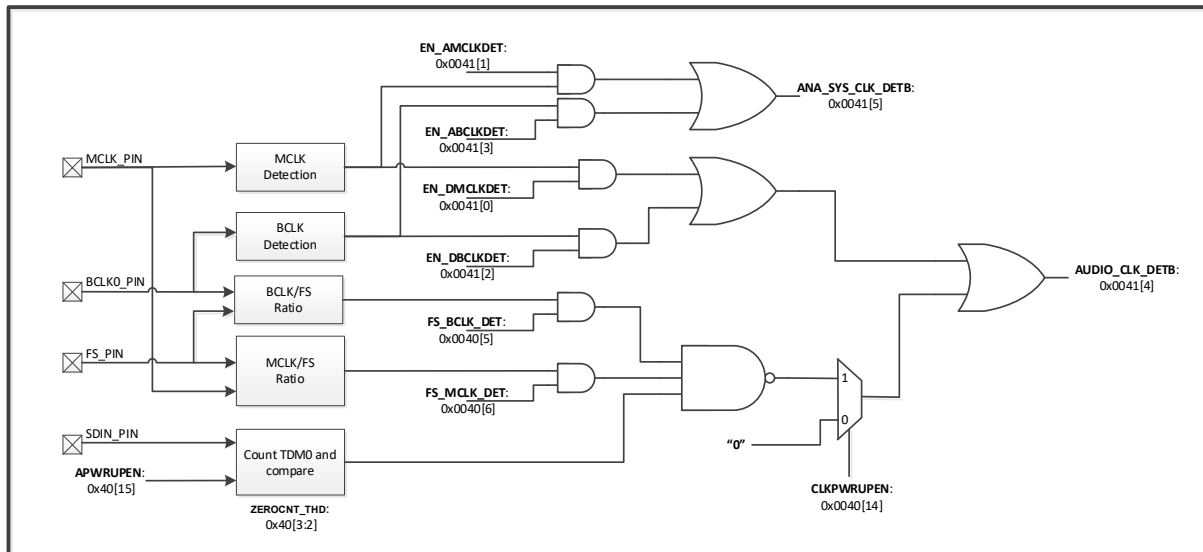


Figure 14 Audio Clock Detection

Register Name	Address	Description / Range
APWRUPEN	0x40[15]	Data non-Zero Counter Enable 1 = Enabled 0 = Disabled
CLKPWRUPEN	0x40[14]	Clock detection Enable. 0 = Disabled 1 = Enabled
REG_SRATE	0x40[12:10]	Audio Sampling rate (FS) setting 000 = 16K 001 = 32K 010 = 48K / 44.1K 011 = 96K 100 = 192K

Register Name	Address	Description / Range
MCLK_RATE	0x40[9:7]	MCLK Frequency setting 000 = 12MHz / 11.025 MHz (44.1 KHz only) 001 = 12.288MHz / 11.2896MHz (44.1 KHz only) 010 = 19.2MHz / 17.64 MHz (44.1 KHz only) 011 = 24MHz / 22.05 MHz (44.1 KHz only) 100 = 24.576MHz / 22.5792MHz (44.1 KHz only)
FS_MCLK_DET	0x40[6]	Enable the MCLK / FS Ratio Detection 1 = Enabled 0 = Disabled
FS_BCLK_DET	0x40[5]	Enable BCLK / FS Ratio Detection 1 = Enabled 0 = Disabled
ZEROCNT_THD	0x40[3:2]	Set the data Zero threshold 00 = 2048 FSYNC 01 = 4096 FSYNC 10 = 8192 FSYNC 11 = 16384 FSYNC

Table 24 Audio Clock Detection Registers

Register Name	Address	Description / Range
ANA_SYS_CLK_DET	0x41[5]	The Analog system clock detection status 0 = Normal 1 = Abnormal
AUDIO_CLK_DET	0x41[4]	The Digital system audio clock detection status 0 = Normal 1 = Abnormal
EN_ABCLKDET	0x41[3]	Enable Analog BCLK Detection 0 = Disabled 1 = Enabled
EN_DBCLKDET	0x41[2]	Enable Digital BCLK Detection 0 = Disabled 1 = Enabled
EN_AMCLKDET	0x41[1]	Enable Analog MCLK Detection 0 = Disabled 1 = Enabled
EN_DMCLKDET	0x41[0]	Enable Digital MCLK Detection 0 = Disabled 1 = Enabled

Table 25 Audio Clock Detection Status Registers

6.9.1 Enabling Audio Clock Detection

Audio Clock Detection in the NAU83G60 is enabled by setting **0x40[14].CLKPWRUPEN** =1'b1, and meeting conditions listed below, depending on the configuration. If all conditions are met, the clock setting of NAU83G60 and Audio path will be configured successfully. If any of the conditions are not met, the Audio path will be disabled.

Conditions for enabling Audio path by Clock Detection:

- If set **0x41[0].EN_DMCLKDET** =1'b1. The NAU83G60 has custom logic Audio Clock Detection circuits that detect if MCLK is present. Only MCLK is present, Audio path can be enabled.
- If set **0x41[2].EN_DBCLKDET** =1'b1. The NAU83G60 has custom logic Audio Clock Detection circuits that detect if BCLK is present. Only BCLK is present, Audio path can be enabled.
- If set **0x40[6].FS_MCLK_DET** =1'b1. Audio Clock Detection logic of NAU83G60 uses **0x40[12:10].REG_SRATE** and **0x40[9:7].MCLK_RATE** to initiate detection of MCLK / FS ratio. The target ratios will be calculated and monitored by NAU83G60 Audio Clock Detection logic. When the detection logic detects a ratio outside the valid ranges, it will assert an invalid MCLK/FS ratio. Only MCLK / FS ratio is correct, Audio path can be enabled.
- If set **0x40[5].FS_BCLK_DET** =1'b1. The NAU83G60 has custom logic Audio Clock Detection circuits that detect if BCLK/FS ratio is correct. Only BCLK/FS ratio is correct, Audio path can be enabled.
- If **0x40[15].APWRUPEN** is set to 1, Audio Clock Detection will require non-zero samples to enable Audio path. Any non-zero sample will be sufficient. After power-up, if zero samples configured in **0x40[3:2].ZEROCNT_THD** are detected, audio path will be disabled. If **0x40[15].APWRUPEN** is set to 0, Audio Clock Detection will not require non-zero samples to enable Audio path.

Audio Clock Detection is suggested to be enabled during normal operation.

6.9.2 Disabling Audio Clock Detection

A Read operation consists of a three-byte Write instruction followed by Read instruction of one or more data bytes. The bus master initiates the operation by issuing the following sequence: a START condition, device address byte with the R/W bit set to "0", and a Control

Audio Clock Detection in the NAU83G60 is disabled by setting **0x40[14].CLKPWRUPEN** to 0. In this state, Audio path is no longer controlled by the enabling conditions listed above, but is set to 1. However, the digital and analog clock detection circuit and clock dividers are still active.

The range of the input clocks is shown in Table 26.

Signal	Min	Max
Frame Synch (FS) (KHz)	16	192
Master Clock MCLK (MHz)	11.025	24.576

Table 26 Range of Input Clocks

6.10 SAR ADC

The SAR ADC is an 12-bit Analog-to-Digital Converter (ADC) used to detect the voltage level on the V_{BAT} supply, and measure the sensor of junction temperature.

6.10.1 SAR ADC Functions

The SAR ADC is enabled by **0x6A[15].SARADC_EN**. Setting this bit to 1 enables the SARADC; setting the bit to 0 disables the function. Before enable SARADC, the SARADC VREF needs to be enabled by setting **0x6B[10].SARADC_VREF_EN** = 1'b1.

Properly setting SARADC average filter and clock divider to get smooth V_{BAT} and T_j Junction Temperature.

Register Name	Address	Description / Range
SARADC_EN	0x6A[15]	SAR_ADC enable 1 = Enable SAR ADC 0 = Disable SAR ADC
SARADC_DIV	0x6A[12]	SARADC CLK divider 1 = CLK_ADC = CLK/2 0 = CLK_ADC = CLK
VBAT_AVG_EN	0x6A[1]	Enable average filter of SAR_ADC VBAT output. 1 = Enable average filter 0 = Disable average filter
VTEMP_AVG_EN	0x6A[0]	Enable average filter of SAR_ADC Temperature sensor output. 1 = Enable average filter 0 = Disable average filter
VTEMP_EN	0x6B[15]	Temperature sensor enable 1 = Enable temperature sensor 0 = Disable temperature sensor
VBATDIV_EN	0x6B[14]	V_{BAT} Divider enable 1 = Enable VBATDIV 0 = Disable VBATDIV
SARADC_VREF_EN	0x6B[10]	SARADC VREF enable 1 = Enable SARADC VREF 0 = VREF_OUT Floating
VTEMP_AVG_N	0x6B[3:2]	Strength VTEMP average filter. 00 = No average 01 = Average 32 data 10 = Average 128 data 11 = Average 512 data
VBAT_AVG_N	0x6B[1:0]	Strength V_{BAT} average filter. 00 = No average 01 = Average 32 data 10 = Average 128 data 11 = Average 512 data

Table 27 SAR ADC Control Registers

6.10.2 SAR ADC Control

The NAU83G60 process and monitor two inputs: Battery Supply Voltage (V_{BAT}) and Junction Temperature (T_j) as shown in Figure 15.

The V_{BAT} divider is enabled by setting **0x6B[14].VBATDIV_EN** = 1'b1. The V_{BAT} voltage can be read out from **0x21[11:0].VBAT_READOUT**. The read out decimal value of **VBAT_READOUT** can be used to calculate the V_{BAT} voltage measured by SARADC by below formula.

$$V_{BAT}(V) = (VBAT_READOUT + 11.08) / 123.53$$

The temperature sensor is enabled by setting **0x6B[15].VTEMP_EN** = 1'b1. The Chip temperature can be read out from **0x22[11:0].TEMP_READOUT**. The read out decimal value of **TEMP_READOUT** can be used to calculate the Junction Temperature measured by SARADC by below formula.

$$T_j(^{\circ}C) = (TEMP_READOUT - 1060.3) / 2.6113$$

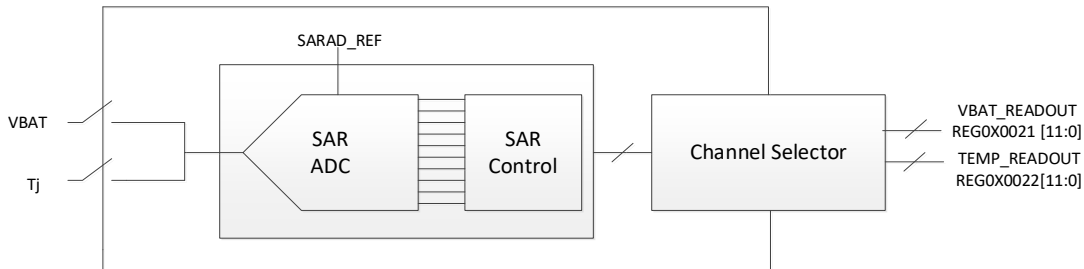


Figure 15 SAR ADC Control

V _{BAT}	SAR VBAT Code	Temp (°C)	SAR T _j Code
5V	25F	-40	48D
6V	2DA	-30	473
7V	356	-20	459
8V	3D1	-10	43E
9V	44D	0	424
10V	4C8	10	40A
11V	544	20	3F0
12V	5BF	30	3D6
13V	63B	40	3BC
14V	6B6	50	3A2
15V	732	60	388
16V	7AD	70	36E
17V	829	80	353
18V	8A4	90	339
19V	920	100	31F
20V	99C	110	305
21V	A17	120	2EB
22V	A93	130	2D1
23V	B0E	140	2B7

V _{BAT}	SAR VBAT Code	Temp (°C)	SAR Tj Code
24V	B8A	150	29D
25V	C05	160	282
26V	C81		

Table 28 SARADC Mapping Table of V_{BAT} And Tj

6.11 Battery Limiter Control

NAU83G60 V_{BAT} has an Over Voltage Lock Out (OVLO) voltage of 27V. If V_{BAT} reaches above this voltage, the class-D driver will shut down and the outputs will remain at ground until the V_{BAT} reaches below the OVLO threshold.

The NAU83G60 V_{BAT} also has an Under Voltage Lock Out (UVLO) voltage of 4.5V. When the battery drops down despite the gain and current limiters, the class-D driver will shut down. If the V_{BAT} drops even further below 1.8V then the device control and registers will reset.

In addition, NAU83G60 employs UVLOP limit threshold (UVLOP_VBAT_THRESHOLD) on the battery voltage V_{BAT}. This limit threshold can be used to program gain changes in order to protect the system from shutting down or to prevent excessive current draw on V_{BAT}. UVLOP limit threshold between UVLO(4.5V) and OVLO(27V) can be programmed in order to adjust the digital gain when the battery voltage drops due to discharge. The UVLOP can reduce the output level in order to reduce the power consumed from the battery supply. See the UVLOP section below for more details. This will prevent large currents from being drawn at low battery voltages as the device tries to supply the load and allow for the battery voltage to recover such that it does not approach the Under Voltage Lockout Threshold (UVLO).

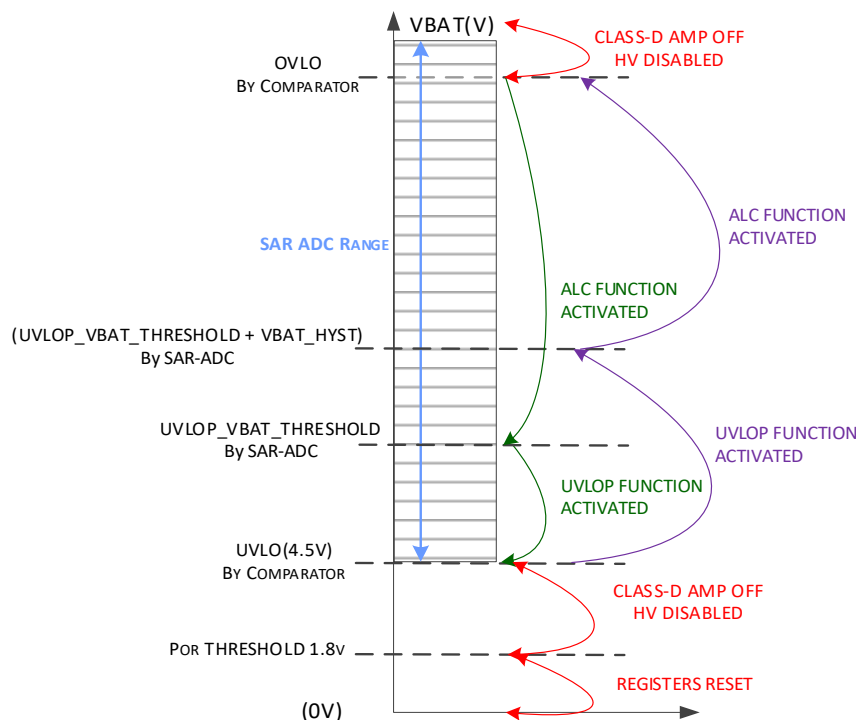


Figure 16 NAU83G60 Battery Limiter Control

6.12 ALC and UVLOP Limiter Mode

The control registers can be reset to default initial conditions. There are two limiter modes supported by NAU83G60 for limiting Class-D output within certain level.

The digital Automatic Level Control (ALC) limiter mode is supported in NAU83G60 by providing an optimized signal level at the output of the Class-D Amplifier. This is achieved by automatically decreasing the gain of the input signal according to the user's set amplitude and restoring gain when conditions are lifted.

The behave of Under Voltage Lock-Out Protection (UVLOP) limiter mode is similar to ALC limiter mode but with V_{BAT} voltage monitor. When low battery voltage is triggered, UVLOP limiter function will automatically decrease the gain of the input signal targeting to the level of user's setting, and restoring gain when conditions are lifted. Please see detail description of UVLOP in 5.12.2 Under Voltage Lockout Prevention (UVLOP) limiter mode operation

ALC and UVLOP limiter have the same mechanism but ALC target level (ALCLVL) has to be set higher than UVLOP target level (UVLOPLVL). The gain limiter of UVLOP can be activated in a faster attack rate than ALC by setting **0x33[1:0].UVLOP_DET_RATE = 2b'11**.

Figure 17 ALC / UVLOP Limiter Block Diagram illustrates the basic relationship of the ALC and UVLOP to other major functions of the NAU83G60.

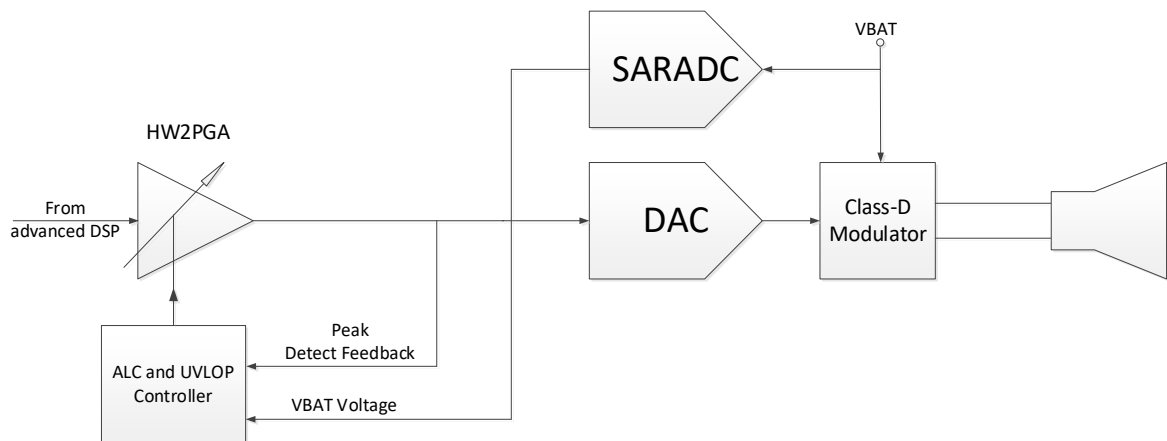


Figure 17 ALC / UVLOP Limiter Block Diagram

6.12.1 Automatic Level Control (ALC) Limiter Mode Operation

The ALC limiter mode is enabled by **0x2E[15].ALCUVLOP_EN** = 1'b1. It detects the peak level of signal output from HW2 Programmable gain amplifier (HW2PGA). Using the output of the HW2PGA provides a direct feedback for ALC controller while using the output of the gain compensation allows for the ALC controller to adjust the gain of HW2PGA based on the activation that is input audio signal level above the user's set amplitude (**ALCLVL**). When activated, ALC controller applies additional attenuation step by step from HW2PGA whose the minimum gain is set by **ALCMINGAIN**. When inactivated, ALC controller removes such additional attenuation step by step from HW2PGA after a period of hold duration.

In the ALC Attack state, the detect interval of peak level is set by **ALCATK**. The HW2PGA decreases the gain step by step gradually at zero cross point of signal.

In the ALC Hold state, the ALC holds constant the HW2PGA gain for a specified time determined by the **ALCHLD** register.

In the ALC Release state, the detect interval of peak level is set by **ALCDCY**. The HW2PGA increases the gain step by step gradually at zero cross point of signal. The gain step of HW2PGA is set by **HW2_VSR**.

The registers below are used for ALC configurations.

- **0x2E[15].ALCUVLOP_EN** - ALC/UVLOP Enable Register, enables the ALC/UVLOP for operation.
- **0x2C[7:5].ALCMAXGAIN** - Set to 3'b111.
- **0x2C[3:1].ALCMINGAIN** - The minimum gain allowed to be set by the ALC on the HW2PGA when enabled to provide additional gain reduction when ALC trigger criterion is fulfilled.
- **0x2D[3:0].ALCLVL** - The target output level of the HW2PGA when ALC active.
- **0x2D[15:12].ALCDCY** - The interval which the ALC detects peak level of HW2PGA output signal to increase the gain in the ALC Release state. The signal determined by step time doubling its increment from 0.5ms to 1024ms with 0.25dB per step. Typically, the decay time is much slower than the attack time.
- **0x2D[11:8].ALCATK** - The interval which the ALC detects peak level of HW2PGA output signal to decrease the gain in the ALC Attack state. The signal determined by step time doubling its increment from 2 μ s to 4196 μ s per step. Typically, the attack time is much faster than the decay time.
- **0x2D[7:4].ALCHLD** - The length of time at which the ALC will hold the gain for, ranging from 0ms to 1024ms. Hold time refers to the duration of time when no action is taken. This is typically used to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU83G60, the hold time value is the duration of time that the DAC output peak value must be less than the target value, ALCLVL, before there is an actual gain increase.

Register Name	Address	Description / Range
ALCMAXGAIN	0x2C[7:5]	Maximum ALC gain setting 111 = 0 dB Others = Reserved
ALCMINGAIN	0x2C[3:1]	Minimum ALC gain setting 000 = -3 dB 001 = -6dB 010 = -9 dB 011 = -12 dB 100 = -16 dB 101 – 111 = Reserved
ALCDCY	0x2D[15:12]	Interval of peak level detection in ALC Release state 0000 = 500 us/step 0001 = 1 ms/step 0010 = 2 ms/step 0011 = 4 ms/step 0100 = 8 ms/step 0101 = 16 ms/step 0110 = 32 ms/step 0111 = 64 ms/step 1000 = 128 ms/step 1001 = 256 ms/step 1010 = 512 ms/step 1011 = 1024 ms/step 1100 – 1111 = Reserved
ALCATK	0x2D[11:8]	Interval of peak level detection in ALC attack state 0000 = 2 μs/step 0001 = 4 μs/step 0010 = 8 μs/step 0011 = 16 μs/step 0100 = 32 μs/step 0101 = 64 μs/step 0110 = 128 μs/step 0111 = 256 μs/step 1000 = 512 μs/step 1001 = 1024 μs/step 1010 = 2048 μs/step 1011 = 4096 μs/step 1100 – 1111 = Reserved
ALCHLD	0x2D[7:4]	Hold time before ALC automated gain increase 0000 = 0 ms 0001 = 2 ms 0010 = 4 ms 0011 = 8 ms 0100 = 16 ms 0101 = 32 ms 0110 = 64 ms 0111 = 128 ms 1000 = 256 ms 1001 = 512 ms 1010 – 1111 = 1024 ms
ALCLVL	0x2D[3:0]	ALC target level 0000 = 0 dBFS 0001 = -1 dBFS 0010 = -2 dBFS 0011 = -3 dBFS 0100 = -4 dBFS 0101 = -5 dBFS 0110 = -6 dBFS 0111 = -7 dBFS 1000 = -8 dBFS 1001 = -9 dBFS 1010 = -10 dBFS 1011 = -11 dBFS 1100 = -12 dBFS 1101 = -13 dBFS 1110 = -14 dBFS 1111 = -15 dBFS
ALCUVLOP_EN	0x2E[15]	0 = ALC/UVLOP Disabled 1 = ALC/UVLOP Enabled

Table 29 ALC Limiter Registers

Please see below sequence as the example of activating ALC Limiter function.

Register Setting Sequence		
Register Name	Value	Description / Range
0x2E[15]	1'b0	ALC/UVLOP Function Disable
0x2C[7:5] 0x2C[3:1]	3'b111 3'b100	ALCMAXGAIN= 0dB ALCMINGAIN= -16dB
0x2D[15:12] 0x2D[11:8] 0x2D[7:4] 0x2D[3:0]	4'b1001 4'b1001 4'b0000 4'b1111	ALCDCY= 256ms/step ALCATK= 1024μs/step ALCHLD= 0ms ALCLVL= -15dBFS
0x2E [15]	1'b1	ALC/UVLOP Function Enable

Table 30 ALC Limiter Function Setting Sequence

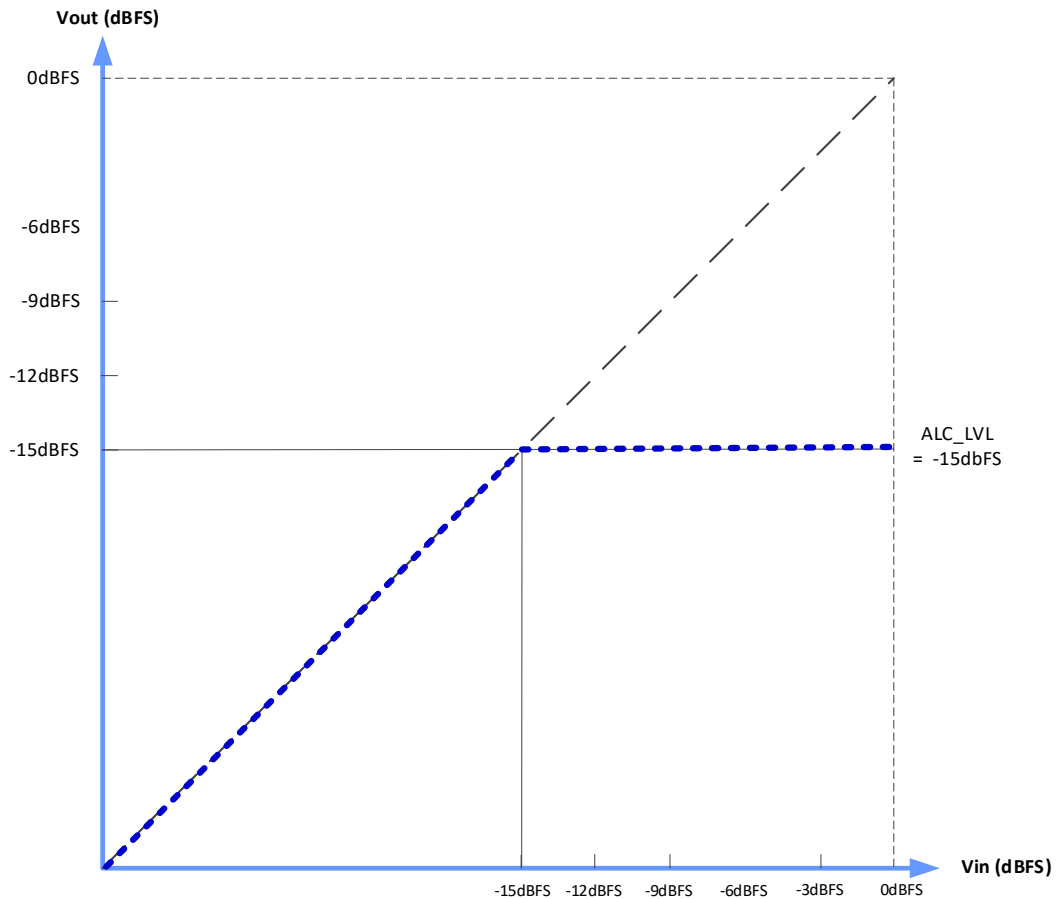


Figure 18 Level Response of ALC Limiter (ALC_LVL=-15dBFS)

6.12.2 Under Voltage Lockout Prevention (UVLOP) Limiter Mode Operation

UVLOP limiter mode has the same output control mechanism as ALC, but activated with monitoring V_{BAT} . UVLOP can configure to faster Attack time by setting **0x33[1:0].UVLOP_DET_RATE** in order to fast response to large currents being drawn at low battery voltages. The UVLOP function is enabled by setting **0x2E[15].ALCUVLOP_EN** =1'b1 with **0x31[15].UVLOP_EN** =1'b1.

NAU83G60 employs UVLOP limit threshold (**UVLOP_VBAT_THRESHOLD**) on the battery voltage V_{BAT} . When $V_{BAT} \geq$ **0x88[11:0].UVLOP_VBAT_THRESHOLD**, the limiter behavior is ALC limiter mode and is applied ALC parameter settings. When $V_{BAT} <$ **0x88[11:0].UVLOP_VBAT_THRESHOLD**, the limiter behavior is UVLOP limiter mode and is applied UVLOP parameter settings. For the mechanism when V_{BAT} recover to the voltage higher than **0x88[11:0].UVLOP_VBAT_THRESHOLD**, the limiter does not switch to ALC limiter mode right away until $V_{BAT} \geq$ (**0x88[11:0].UVLOP_VBAT_THRESHOLD + 0x33[15:4].UVLOP_VBAT_HYST**).

UVLOP limiter mode detects the peak level of signal output from HW2 Programmable gain amplifier (HW2PGA). Using the output of the HW2PGA provides a direct feedback for control while using the gain compensation allows for the UVLOP controller to adjust based on the activation that is input audio signal level above the user's set amplitude (**UVLOPLVL**). When activated, UVLOP controller apply additional attenuation step by step whose the minimum gain is set by **UVLOPMINGAIN**. When inactivated, UVLOP controller removes such additional attenuation step by step after a period of hold duration.

In the UVLOP Attack state, the detect interval of peak level is set by **UVLOPATK**. The HW2PGA decreases the gain step by step gradually at zero cross point of signal.

In the UVLOP Hold state, the UVLOP holds constant the HW2PGA gain for a specified time determined by the **UVLOPHLD** register.

In the UVLOP Release state, the detect interval of peak level is set by **UVLOPDCY**. The HW2PGA increases the gain step by step gradually at zero cross point of signal. The gain step of HW2PGA is set by **HW2_VSR**.

The registers below are used for UVLOP configurations.

- **0x2E[15].ALCUVLOP_EN** - ALC/UVLOP Enable Register, enables the ALC/UVLOP for operation.
- **0x31[15].UVLOP_EN** - UVLOP Enable Register, enables the UVLOP for operation.
- **0x88[11:0].UVLOP_VBAT_THRESHOLD** - UVLOP Activate Register, when V_{BAT} is measured under V_{BAT} threshold of UVLOP, the gain adjustment from HW2PGA will be activated.
- **0x31[7:5].UVLOPMAXGAIN** - Set to 3'b111.
- **0x31[3:1].UVLOPMINGAIN** - The minimum gain level allowed to be set by the UVLOP on the HW2PGA when enabled to provide additional gain reduction when UVLOP trigger criterion is fulfilled.
- **0x32[15:12].UVLOPDCY** - The interval which the UVLOP detects peak level of HW2PGA output signal to increase the gain in the UVLOP Release state. The signal determined by step time doubling its increment from 500 μ s to 1024ms at 0.25dB per step. Typically, the decay time is much slower than the attack time.
- **0x32[11:8].UVLOPATK** - The interval which the UVLOP detects peak level of HW2PGA output signal to decrease the gain in the UVLOP Attack state. The signal determined by step time doubling its increment from 2 μ s to 4096 μ s at 0.25dB per step. Typically, the attack time is much faster than the decay time.
- **0x32[7:4].UVLOPHLD** - The length of time at which the UVLOP will hold the gain for, ranging from 0ms to 1024ms. Hold time refers to the duration of time when no action is taken. This is typically used to avoid undesirable sounds that can happen when an UVLOP responds too quickly to a changing input signal. In the NAU83G60, the hold time value is the duration of time that the DAC output peak value must be less than the target value, **UVLOPLVL**, before there is an actual gain increase.
- **0x32[3:0].UVLOPLVL** - The target output level of the HW2PGA when UVLOP active.

In order to avoid conflict between ALC and UVLOP function, please set ALCLVL level > UVLOPLVL level.

Register Name	Address	Description / Range
ALCUVLOP_EN	0x2E[15]	0 = ALC/Limiter Disabled (fixed gain) 1 = ALC/Limiter Enabled
UVLOP_EN	0x31[15]	0 = UVLOP/Limiter Disabled (fixed gain) 1 = UVLOP/Limiter Enabled (Please make sure 0x2E[15].ALC_EN = 1'b1 when set UVLOP_EN = 1'b)
UVLOPMAXGAIN	0x31[7:5]	Maximum UVLOP gain setting 111 = 0 dB Others = Reserved
UVLOPMINGAIN	0x31[3:1]	Minimum UVLOP gain setting 000 = -3 dB 001 = -6dB 010 = -9 dB 011 = -12 dB 100 = -16 dB 101 – 111 = Reserved
UVLOPCY	0x32[15:12]	Interval of peak level detection in UVLOP Release state 0000 = 500 μ s/step 0001 = 1 ms/step 0010 = 2 ms/step 0011 = 4 ms/step 0100 = 8 ms/step 0101 = 16 ms/step 0110 = 32 ms/step 0111 = 64 ms/step 1000 = 128 ms/step 1001 = 256 ms/step 1010 = 512 ms/step 1011 = 1024 ms/step 1100 – 1111 = Reserved
UVLOPATK	0x32[11:8]	Interval of peak level detection in UVLOP attack state 0000 = 2 μ s/step 0001 = 4 μ s/step 0010 = 8 μ s/step 0011 = 16 μ s/step 0100 = 32 μ s/step 0101 = 64 μ s/step 0110 = 128 μ s/step 0111 = 256 μ s/step 1000 = 512 μ s/step 1001 = 1024 μ s/step 1010 = 2048 μ s/step 1011 = 4096 μ s/step 1100 – 1111 = Reserved
UVLOPHLD	0x32[7:4]	Hold time before UVLOP automated gain increase 0000 = 0 ms 0001 = 2 ms 0010 = 4 ms 0011 = 8 ms 0100 = 16 ms 0101 = 32 ms 0110 = 64 ms 0111 = 128 ms 1000 = 256 ms 1001 = 512 ms 1010 – 1111 = 1024 ms

Register Name	Address	Description / Range
UVLOPLVL	0x32[3:0]	UVLOP target level 0000 = 0 dBFS 0001 = -1 dBFS 0010 = -2 dBFS 0011 = -3 dBFS 0100 = -4 dBFS 0101 = -5 dBFS 0110 = -6 dBFS 0111 = -7 dBFS 1000 = -8 dBFS 1001 = -9 dBFS 1010 = -10 dBFS 1011 = -11 dBFS 1100 = -12 dBFS 1101 = -13 dBFS 1110 = -14 dBFS 1111 = -15 dBFS
UVLOP_VBAT_HYST	0x33[15:4]	V _{BAT} Hysteresis voltage of UVLOP Dec2Hex [Round(123.53 * UVLOP_VBAT_HYST)]
UVLOP_DET_RATE	0x33[1:0]	UVLOP Audio Signal Detect RATE 00 = Slow 01 = Reserved 10 = Reserved 11 = Fast
UVLOP_VBAT_THRESHOLD	0x88[11:0]	UVLOP Threshold voltage set Dec2Hex [Round(123.53 * VBAT_THD2 - 11.08)]

Table 31 UVLOP Limiter Mode Registers

Please see below sequence as the example of activating ALC Limiter function.

Register Setting Sequence		
Register Name	Value	Description / Range
0x2D[3:0]	3'b000	ALC_LVL= 0 dBFS; set ALCLVL level > UVLOPLVL level
0x2E [15]	1'b1	ALC/UVLOP function enable
0x32[15:12]	4'b1001	UVLOPDCY= 256ms/step
0x32[11:8]	4'b1001	UVLOPATK= 1024μs/step
0x32[7:4]	4'b0000	UVLOPHLD= 0ms
0x32[3:0]	4'b1111	UVLOPLVL= -15dBFS
0x33[1:0]	2'b11	UVLOP_DET_RATE=Fast
0x33[15:4]	12'h173	UVLOP_VBAT_HYST=3V
0x88[11:0]	12'h920	UVLOP_VBAT_THR= 19V
0x31[7:5]	3'b111	UVLOPMAXGAIN= 0dB
0x31[3:1]	3'b100	UVLOPMINGAIN= -16dB
0x31[15]	1'b1	UVLOP enable

Table 32 UVLOP Limiter Function Setting Sequence

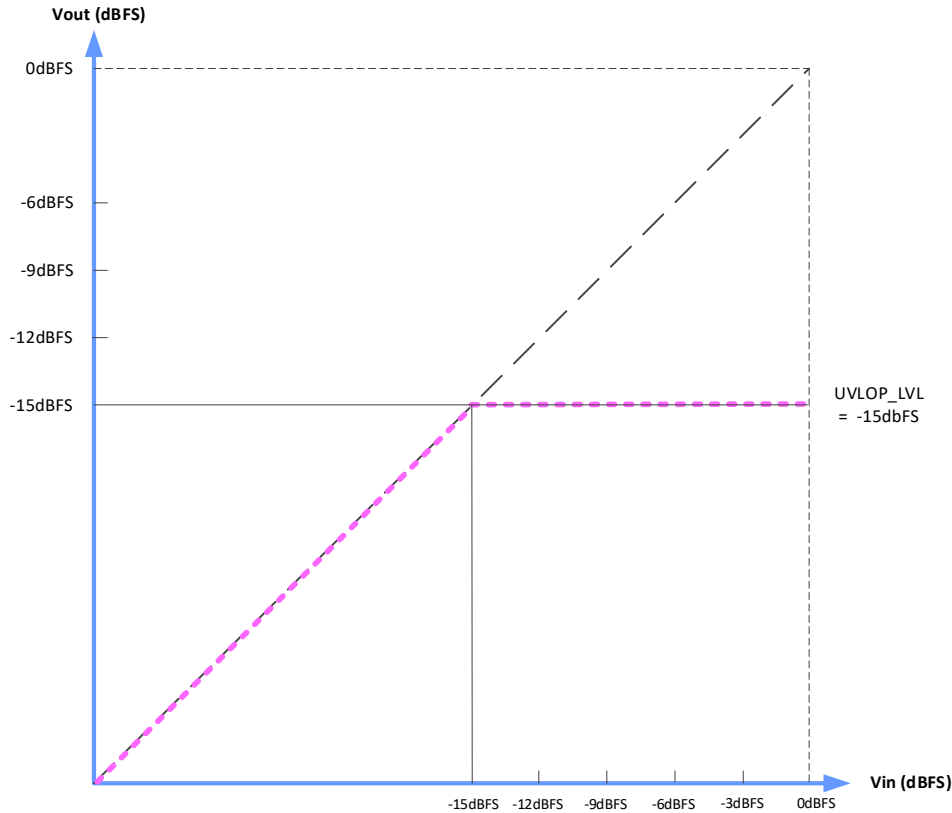


Figure 19 Level Response of UVLOP Limiter Triggered When V_{BAT} Reaches Threshold (UVLOP_LVL=-15dBFS)

6.13 Device Protection

The NAU83G60 includes the following types of device protection when fault event is detected:

- Short Current Protection (SCP)
- Supply Over Voltage Lock Out (OVLO)
- Under Voltage Lock Out (UVLO)
- Over Temperature Protection (OTP)
- Clock Termination Protection (CTP)

Short Current Protection (SCP) is provided in the NAU83G60. If a short circuit is detected on any of the shortage between power stage output and GND or V_{BAT} , the output drivers will be disabled. The output drivers will be enabled after short circuit is removed.

Supply Over Voltage Lock Out (OVLO) is provided in the NAU83G60. If the V_{BAT} supply voltage reaches 27V, the output drivers will be set to pull down to ground while the NAU83G60 control circuitry continues to operate. If the supply drops below 26V, the output drivers are re-enabled.

Under Voltage Lock Out (UVLO) provides Supply Under Voltage Protection in the NAU83G60. If the V_{BAT} supply voltage drops below 4.5V, the output drivers will be disabled while the NAU83G60 control circuitry continues to operate. This will prevent the battery supply from going too low before the host processor can safely shut down the devices on the system. If the supply goes back up, the drivers will be enabled again at 4.8V. If the supply drops further below 1.8V, the internal power-on reset is activated and puts the entire device into the power-down state.

Over Temperature Protection (OTP) is provided in the event of thermal overload. When the internal junction temperature of the device is too high (145 °C), the NAU83G60 will disable the output drivers. When the device cools down and a safe operating temperature (15 °C hysteresis) has been achieved, the output drivers will be enabled again.

Clock Termination Protection (CTP) is provided in the NAU83G60. If the clock stops running, the NAU83G60 automatically shuts down the Class-D driver if Audio Clock Detection is enabled. Refer to 5.9Audio Clock Detection.

All detected fault events are recorded and related interrupt can be configured to inform Host for further process. Refer to section 6.9 Interrupt Request.

6.14 Digital Serial Control Interface

Command and control of the device are accomplished by using I2C. The NAU83G60 includes a 2-wire interface (I2C) as slave device that provides access to all of the device control registers. The I2C control interface provides a flexible, 2-wire Serial Control Interface and its Max clock is up to 1MHz to reduce the initialization time during the system power on. The NAU83G60 provides I2C address selection depending on the state of GPIO1/GPIO2 pins.

The I2C Device address of NAU83G60 can be configured to 0x1A, 0x1B, 0x4A or 0x4B when power on by external pull up or pull down to GPIO1 and GPIO2 pin status as below table. Write **0x02[0].I2C_ADDR_LCH** to 1 latches I2C Device Address.

Register Name	Address	Description / Range
I2C_ADDR_LCH	0x2[0]	Write 1 To Latch the I2C Device Address
DEVICE ID	0x46[14:8]	According to the External Pull Up or Pull Down to Define The I2C Device Address. Pull Down GPIO2, Pull Down GPIO1 => 1A Pull Down GPIO2, Pull Up GPIO1 => 1B Pull Up GPIO2, Pull Down GPIO1 => 4A Pull Up GPIO2, Pull Up GPIO1 => 4B

Table 33 I2C Device Address Registers

6.14.1 2-Wire-Serial Control Mode (I2C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU83G60 can function only as a slave device when in the 2-wire interface configuration.

6.14.2 2-Wire Protocol Convention

To initiate communication, all 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. Following a START condition, the master must output a device address byte consisting of a 7-bit device address, and a Read/Write control bit in the LSB of the address byte. To read from the slave device, the R/W bit must be set to 1. To initiate a write to the slave device, the R/W bit must be 0. If the device address matches the address of a slave device, the slave will output an acknowledgement bit.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits and during the ninth clock cycle, the receiver (slave) pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

To terminate a read/write session, all 2-Wire interface operations must end with a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

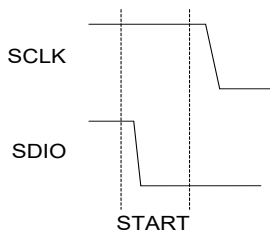


Figure 20 Valid START condition

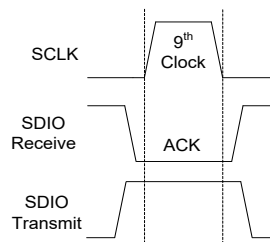


Figure 21 Valid Acknowledge

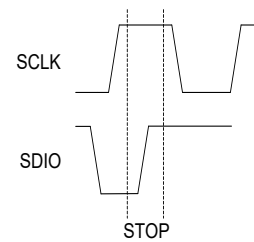


Figure 22 Valid STOP Condition

6.14.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more data bytes as seen in Figure 23. These instructions consist of the Address byte and two Control Address bytes that precede the START condition and are followed by the STOP condition. Figure 24 shows the data bus and the corresponding clock cycles.

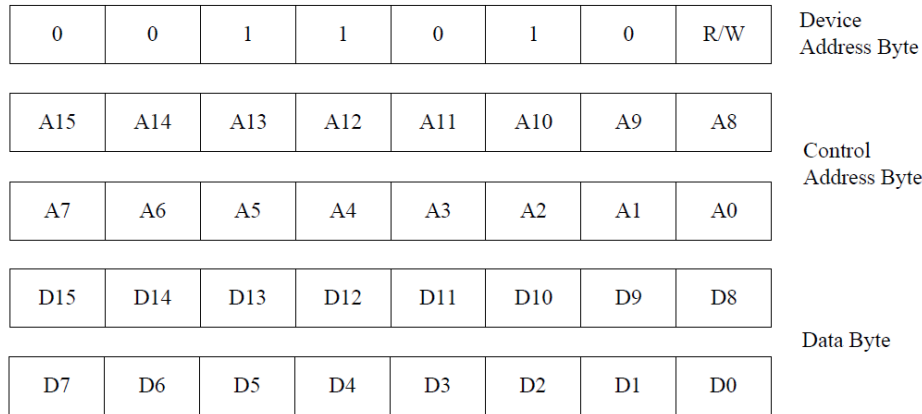


Figure 23 Slave Address Byte, Control Address Byte and Data Byte

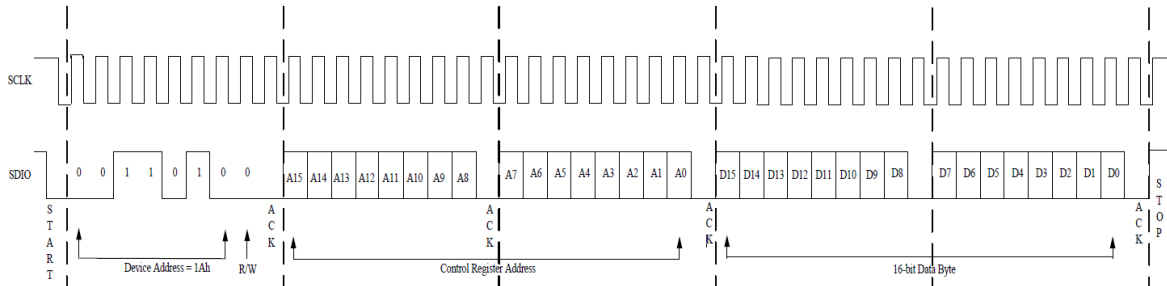


Figure 24 Two-Wire Write Sequence

6.14.4 2-Wire Read Operation

A Read operation consists of the three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, Device Address byte with the R/W bit set to “0” , and a Control Register Address byte. This indicates to the NAU83G60 which of its control registers is going to be accessed.

After this, the NAU83G60 will respond with an ACK as it accepts the Control Register Address that the master is transmitting to it. After the Control Register Address has been sent, the master will send a second START condition and Device address but with R/W = 1.

After the NAU83G60 recognizes its Device Address the second time, it will transmit an ACK followed by a two byte value containing the 16 bits of data in the NAU83G60 control registers requested by the master. During this phase, the master generates an ACK with each byte of data transferred.

After the two bytes have been transmitted, the master will send a STOP condition ending the read phase. If no STOP condition is received, the NAU83G60 will automatically increment the target Control Register

Address and then start sending the two bytes of data for the next register in the sequence. This will continue as long as the master continues to send ACK signals. Once the target register reaches 0xFFFF, it will send the associated data then roll over to 0x00 and continue as before

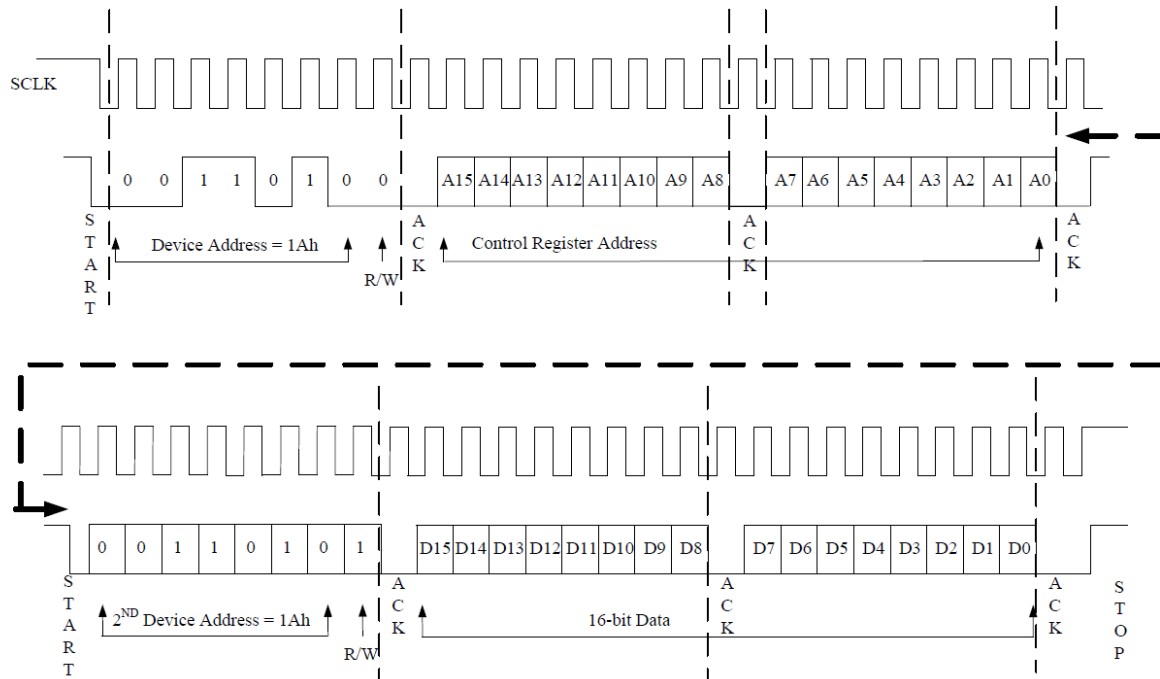


Figure 25 Two-Wire Read Sequence

6.14.5 Digital Serial Control Interface Timing

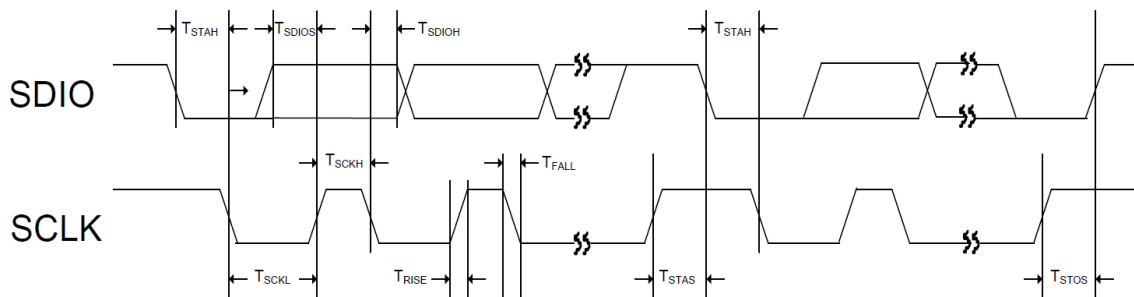


Figure 26 Two-wire Control Mode Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T _{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	---	---	ns
T _{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600			ns
T _{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600			ns
T _{SCKH}	SCLK High Pulse Width	600			ns
T _{SCKL}	SCLK Low Pulse Width	1,300			ns
T _{RISE}	Rise Time for all 2-wire Mode Signals			300	ns
T _{FALL}	Fall Time for all 2-wire Mode Signals			300	ns
T _{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100			ns
T _{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time			600	ns

Table 34 Two-wire Control Mode Timing Parameters

6.15 Digital Audio Interface

The TDM Interface is the main audio interface of NAU83G60. TDM transmit path can be enable/disable by **0x0B[15].EN_TDM_TX** while receive path can be enable/disable by **0x0B[14].EN_TDM_RX**. TDM interface is designed as Slave mode. The channel length set by **0x0C[9:8].TDM_CLEN** decides how many bits is set as a channel while the data length set by **0x0C[11:10].TDM_DLEN** decides how many bits of audio data in one channel is processed. The channel length needs to be set larger than data length. The NAU83G60 supports four port data lengths: 16, 20, 24, and 32 bits. **0x0B[8].FRAME_START** sets the polarity of TDM Interface. In addition, configure **0x0C[15].TDM_SDO_PU** and **0x0C[14].TDM_SDO_PD** to enable/disable pull-up or pull-down function of SDOOUT pin.

Set **0x0B[7].RX_JUSTIFY=1'b1** to enable Right Justify format.

Register Name	Address	Description / Range
EN_TDM_TX	0x0B[15]	TDM TX Enable 0 = Disabled 1 = Enabled
EN_TDM_RX	0x0B[14]	TDM RX Enable 0 = Disabled 1 = Enabled
FRAME_START	0x0B[8]	TDM Frame Start Polarity 0 = Frame Start When FSYNC Change from Low to High 1 = Frame Start When FYSNC Change from High to Low
RX_JUSTIFY	0x0B[7]	TDM RX Left / Right Justified Select 0 = Left Justify 1 = Right Justify

Register Name	Address	Description / Range
TDM_SDO_PU	0x0C[15]	TDM SDO Pin Pull-Up Enable 0 = Floating 1 = Pull-Up TDM SDO
TDM_SDO_PD	0x0C[14]	TDM SDO Pin Pull-Down Enable 0 = Floating 1 = Pull-Up TDM SDO
TDM_DLEN	0x0C[11:10]	Data Length Of TDM 00 = 16 Bits 01 = 20 Bits 10 = 24 Bits 11 = 32 Bits
TDM_CLEN	0x0C[9:8]	Channel Length Of TDM 00 = 16 Bits 01 = 24 Bits Others = 32 Bits

Table 35 Digital Audio Interface General Format Registers

The TDM Interface of NAU83G60 supports nine audio formats: I2S, Right Justified, Left Justified, TDM-I2S, TDM-Right Justified, TDM-Left Justified, PCM A, PCM B and PCM Offset. When operated in the TDM-I2S, TDM-Right Justified, or TDM-Left Justified mode and in all PCM modes, the NAU83G60 supports up to 8-channel data transmission on both ADC and DAC paths simultaneously. The supported Channel lengths, Sample rates are listed below with BCLK frequency requirement.

CH No. =	2			DSP FS (KHz)
Channel length	16	24	32	
FS (KHz)	BCLK (MHz)			
16	0.512	0.768	1.024	48
32	1.024	1.536	2.048	48
48	1.536	2.304	3.072	48
96	3.072	4.608	6.144	48
192	6.144	9.216	12.288	48

CH No. =	2			DSP FS (KHz)
Channel length	16	24	32	
FS (KHz)	BCLK (MHz)			
14.7	0.4704	0.7056	0.9408	44.1
29.4	0.9408	1.4112	1.8816	44.1
44.1	1.4112	2.1168	2.8224	44.1
88.2	2.8224	4.2336	5.6448	44.1
176.4	5.6448	8.4672	11.2896	44.1

CH No. =	4			DSP FS (KHz)
Channel length	16	24	32	
FS (KHz)	BCLK (MHz)			
16	1.024	1.536	2.048	48
32	2.048	3.072	4.096	48
48	3.072	4.608	6.144	48
96	6.144	9.216	12.288	48
192	12.288	18.432	24.576	48

CH No. =	4			DSP FS (KHz)
Channel length	16	24	32	
FS (KHz)	BCLK (MHz)			
14.7	0.9408	1.4112	1.8816	44.1
29.4	1.8816	2.8224	3.7632	44.1
44.1	2.8224	4.2336	5.6448	44.1
88.2	5.6448	8.4672	11.2896	44.1
176.4	11.2896	16.9344	22.5792	44.1

CH No. =	8			DSP FS (KHz)
Channel length	16	24	32	
FS (KHz)	BCLK (MHz)			
16	2.048	3.072	4.096	
32	4.096	6.144	8.192	48
48	6.144	9.216	12.288	48
96	12.288	18.432	24.576	48
192	24.576			48

CH No. =	8			DSP FS (KHz)
Channel length	16	24	32	
FS (KHz)	BCLK (MHz)			
14.7	1.8816	2.8224	3.7632	44.1
29.4	3.7632	5.6448	7.5264	44.1
44.1	5.6448	8.4672	11.2896	44.1
88.2	11.2896	16.9344	22.5792	44.1
176.4	22.5792			44.1

Table 36 Supported Channel Length and Sample Rates of Digital Audio Interface

The NAU83G60 has two Audio DAC channels and four ADC channels for I_{Sense} and V_{Sense} . Every input signal of Audio DAC (Audio Input and ANC Input) can be assigned to different TDM RX time slot. Every output signal of I_{VSense} ADC and SARADC data signal measured from V_{BAT} and Junction Temperature can be assigned to different TDM TX time slot. Also Advanced DSP processed audio signal can be assigned to different TDM TX time slot and transmitted through TDM TX as reference signal of Acoustic Echo Cancellation (AEC).

For Receive path (RX path) which Host send audio data to NAU83G60, **0x0B[6:2].RX_OFFSET** sets the BCLK cycles between frame start (FS transition) and first RX slot0. Audio Right/Left channel data and ANC Right/Left channel data can be assign to different slot by registers list below:

For Transmission path (TX path), NAU83G60 can send not only audio data but also some of the internal signal data to Host, **0x0D[11:9].TX_OFFSET** sets the BCLK cycles between frame start (FS transition) and first TX slot (slot0).

Audio PDM Right/Left channel data, I_{Sense} Right/Left data, V_{Sense} Right/Left data, AEC reference Right/Left channel data, ANC Right/Left channel data, Junction Temperature (T_j) measured data and V_{BAT} measured data can be assign to different slot by registers list below:

Register Name	Address	Description / Range
RX_Audio_R	0x0C[7:4]	TDM RX Audio Right Channel Time Slot
RX_Audio_L	0x0C[3:0]	TDM RX Audio Left Channel Time Slot
RX_ANC_R	0x10[15:12]	TDM RX ANC Right Channel Time Slot
RX_ANC_L	0x10[11:8]	TDM RX ANC Left Channel Time Slot
RX_Offset	0x0B[6:2]	RX Offset, BCLK Cycles In Between Frame Start (Fsync Transition) To Slot0
TX_OFFSET	0x0D[11:9]	BCLK Count In Between FSYNC Start and First TX Slot (Slot0)
TJ_TX_EN	0x10[6]	TX Temp Enable 0 = Disabled 1 = Enabled
TJ_SLOT	0x10[5:0]	TDM TX Temp Time Slot
VBAT_TX_EN	0x0F[14]	TDM TX V_{BAT} Transmit Enable 0 = Disabled 1 = Enabled
VBAT_SLOT	0x0F[13:8]	TDM TX V_{BAT} time slot
PDM_L_SLEN	0x0E[7]	PDM Left Channel Sample Slot Length of TDM TX 0 = 16-Bits 1 = 32-Bits
PDM_TX_L_EN	0x0E[6]	PDM Left Channel Data to TDM TX Transmit Enable 0 = Disabled 1 = Enabled
PDM_L_SLOT	0x0E[5:0]	PDM Left Channel Time Slot of TDM TX
PDM_R_SLEN	0x0F[7]	PDM Right Channel Sample Slot Length of TDM TX 0 = 16-bits 1 = 32-bits

Register Name	Address	Description / Range
PDM_TX_R_EN	0x0F[6]	PDM Right Channel Data to TDM TX transmit enable 0 = Disabled 1 = Enabled
PDM_R_SLOT	0x0F[5:0]	PDM right channel time slot of TDM TX
VSNS_R_SLEN	0x11[15]	TDM TX V _{Sense} Right Channel Slot Length 0 = 8-bits 1 = 16-bits
VSNS_R_TX_EN	0x11[14]	TDM TX V _{Sense} R Enable 0 = Disabled 1 = Enabled
VSNS_R_SLOT	0x11[13:8]	TDM TX V _{Sense} R slot
VSNS_L_SLEN	0x0D[7]	TDM TX V _{Sense} Left Channel Slot Length 0 = 8-Bits 1 = 16-Bits
VSNS_L_TX_EN	0x0D[6]	TDM TX V _{Sense} L Enable 0 = Disabled 1 = Enabled
VSNS_L_SLOT	0x0D[5:0]	TDM TX Voltage Sense Time Slot
ISNS_L_SLEN	0x0E[15]	TDM TX I _{Sense} Left Channel Slot Length 0 = 8-Bits 1 = 16-Bits
ISNS_L_TX_EN	0x0E[14]	0 = Disable Transmission of Current Sense Data 1 = Enable Transmission of Current Sense Data
ISNS_L_SLOT	0x0E[13:8]	TDM TX Current Sense Time Slot
ISNS_R_SLEN	0x11[7]	TDM TX I _{Sense} Right Channel Slot Length 0 = 8-bits 1 = 16-bits
ISNS_R_TX_EN	0x11[6]	TDM TX I _{Sense} R Enable 0 = Disabled 1 = Enabled
ISNS_R_SLOT	0x11[5:0]	TDM TX I _{Sense} R slot
AEC_L_TX_SLEN	0x17[15]	TDM TX AEC L-CH Slot Length 0 = 16-bit 1 = 32-bit
AEC_L_TX_EN	0x17[14]	TDM TX AEC L-CH Enable 0 = Disabled 1 = Enabled
AEC_L_TX_SLOT	0x17[13:8]	TDM TX AEC L-CH Slot
AEC_R_TX_SLEN	0x17[7]	TDM TX AEC R-CH Slot Length

Register Name	Address	Description / Range
		0 = 16-bits 1 = 32-bits
AEC_R_TX_EN	0x17[6]	TDM TX AEC R-CH Enable 0 = Disabled 1 = Enabled
AEC_R_TX_SLOT	0x17[5:0]	TDM TX AEC R-CH Slot

Table 37 TDM RX/TX Channel Slot and Format Control Registers

Slot setting is the same concept in different signal, below use AEC signal as example:

Setting **0x17[5:0].AEC_R_TX_SLOT** =5b'00100 can put AEC right channel data on 2nd channel of TDM TX when TDM TX channel length is 32 Bits.

Setting **0x17[5:0].AEC_R_TX_SLOT** =5b'00010 can put AEC right channel data on 2nd channel of TDM TX when TDM TX channel length is 16 Bits.

Please note that the Unit of slot is in byte.

Below sections make more description to some of popular audio formats.

6.15.1 TDM-Left-Justified Audio Data

Left-Justified Mode is configured by setting **0x0B[6:2].RX_OFFSET** = 5'b00000, **0x0D[11:9].TX_OFFSET** = 3'b000, **0x0B[7].RX_JUSTIFY** = 1'b1. When Audio clock detected more than two PCM data slot within a FS cycle. User need to arrange different transmitted or received PCM data to different slot.

When **0x0B[8].FRAME_START** = 1'b0, the MSB is clocked on the first BCLK rising edge after the FS transitions.

When in Left-Justified Mode, FS is HIGH, Channel 0 data is transmitted; when FS is LOW, Channel 1 data is transmitted. This can be seen in Figure 27.

When in TDM-Left-Justified Mode, FS is HIGH, Channel 0 data is transmitted, then Channel 2, 4, and 6 data are transmitted; when FS is LOW, Channel 1 data is transmitted then Channel 3, 5, and 7 data are transmitted. This can be seen in Figure 28.

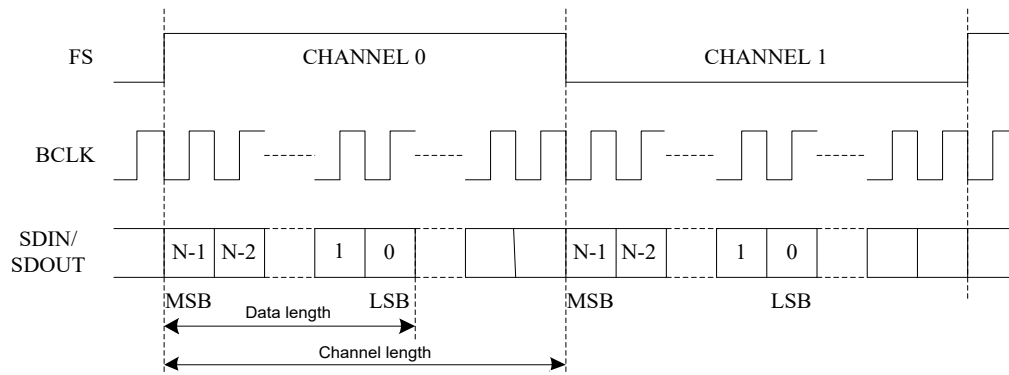


Figure 27 Left-Justified Audio Data

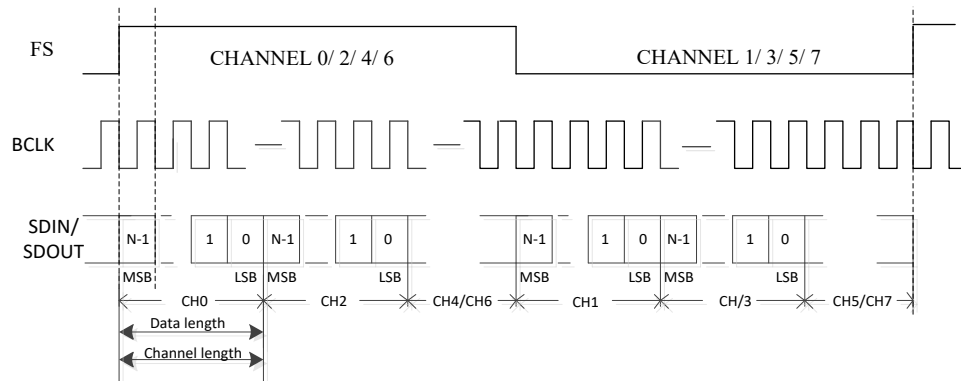


Figure 28 TDM- Left-Justified Audio Data

6.15.2 TDM-I2S Audio Data

I2S Mode is configured by setting **0x0B.RX_OFFSET[6:2] = 5'b00001**, **0x0D[11:9].TX_OFFSET = 3'b001**, **RX_JUSTIFY(REG0x0B[7]) = 1'b0**. When Audio clock detected more than two PCM data slot within a FS cycle. User need to arrange transmitted/received PCM data to different slot.

When **0x0B[8].FRAME_START = 1'b1**, the MSB is clocked on the second BCLK rising edge after the FS transitions.

When in I2S Mode, FS is LOW, Left Channel data is transmitted; when FS is HIGH, Right Channel data is transmitted. This can be seen in Figure 29.

When in TDM-I2S Mode, FS is LOW, Channel 0 data is transmitted then Channel 2, 4, and 6 data are transmitted; when FS is HIGH, Channel 1 data is transmitted then Channel 3, 5, and 7 data are transmitted. This can be seen in Figure 30.

Note: In standard I2S mode the V_{Sense} channel has one sample delay with respect to the I_{Sense} channel.

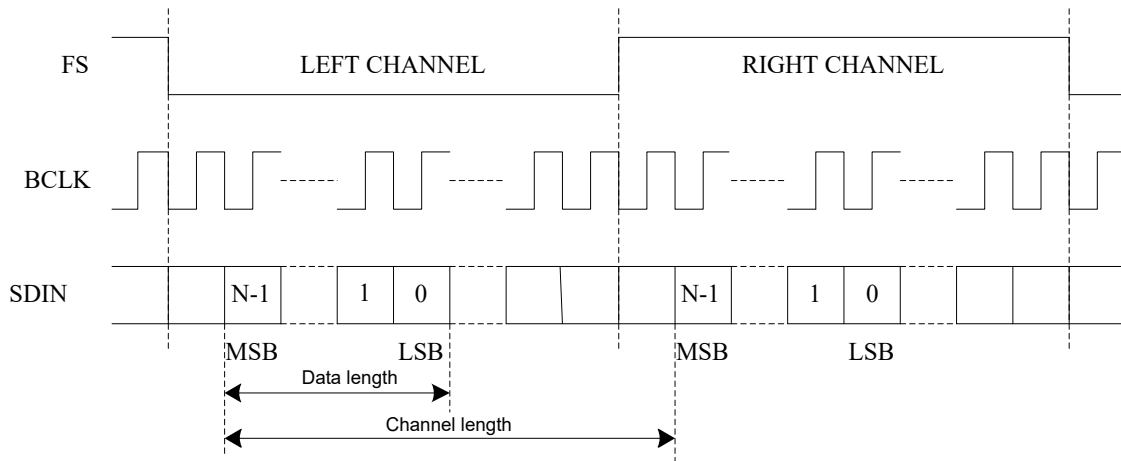


Figure 29 I2S Audio Data

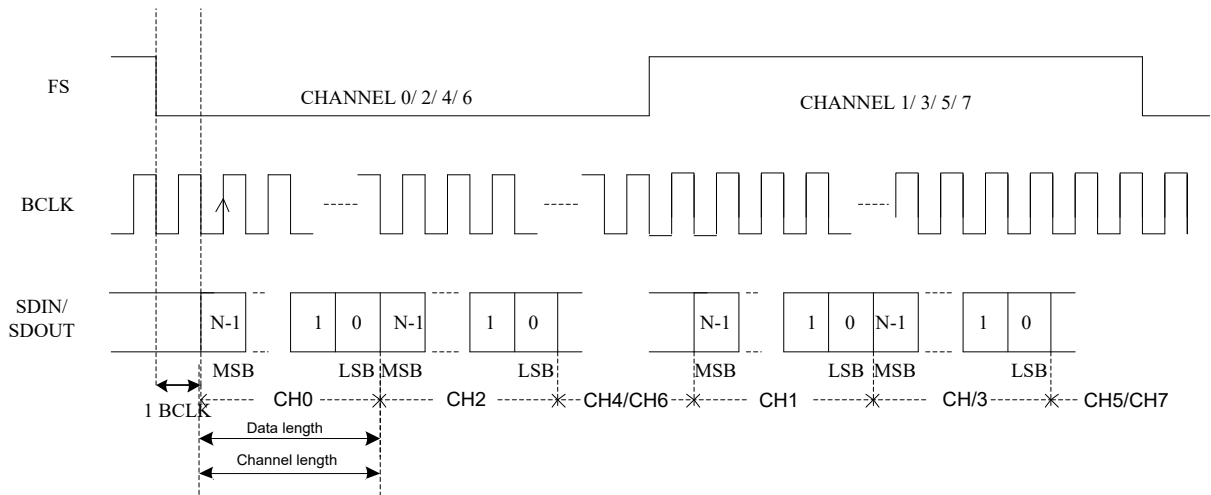


Figure 30 TDM-I2S Audio Data

6.15.3 PCM A Time Slot Audio Data

PCM A Mode is configured by setting **0x0B[8].FRAME_START=1'b0**, **0x0B[6:2].RX_OFFSET=5'b00001**, **0x0D[11:9].TX_OFFSET=3'b001**, **0x0B[7].RX_JUSTIFY=1'b0**. When Audio clock detected more than two PCM data slot within a FS cycle. User need to arrange transmitted/received PCM data to different slot.

In PCM A Mode, Channel 0 data are transmitted first, followed sequentially by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. Channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in Figure 31. Note that this supports only 8 channels as shown here.

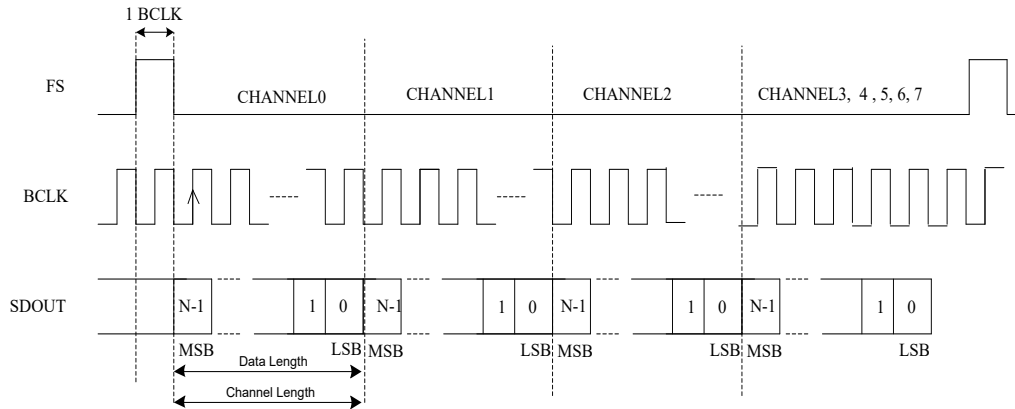


Figure 31 PCM A Time Slot Audio Data

6.15.4 PCM B Time Slot Audio Data

PCM B Mode is configured by setting **0x0B[8].FRAME_START=1'b0**, **0x0B[6:2].RX_OFFSET=5'b00000**, **0x0D[11:9].TX_OFFSET=3'b000**, **0x0B[7].RX_JUSTIFY=1'b0**. When Audio clock detected more than two PCM data slot within a FS cycle. User need to arrange transmitted/received PCM data to different slot.

In PCM B Mode, Channel 0 data are transmitted first, followed immediately by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the Channel 1 MSB is clocked on the next SCLK after the Channel 0 LSB. This is shown in Figure 32.

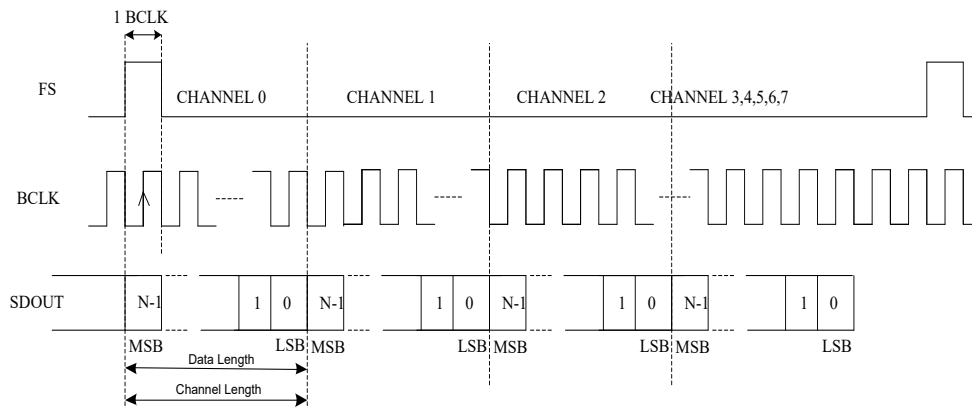


Figure 32 PCM B Time Slot Audio Data

6.15.5 PCM Time Offset Audio Data

PCM Time Offset Mode is used to delay the time at which the DAC and/or ADC data are clocked. This increases the flexibility of the NAU83G60 for use in a wide range of system designs. One key application of this feature is to enable multiple NAU83G60 chips or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS). In this mode, audio data are delayed by a delay count specified in the device control registers. PCM Time Offset Mode typically set **0x0B[8].FRAME_START=1'b0**. Channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in **0x0B[6:2].RX_OFFSET** for TDM RX or **0x0D[11:9].TX_OFFSET** for TDM TX. The subsequent channel's MSB is clocked on the next BCLK after the LSB of the previous channel. This can be seen in Figure 33.

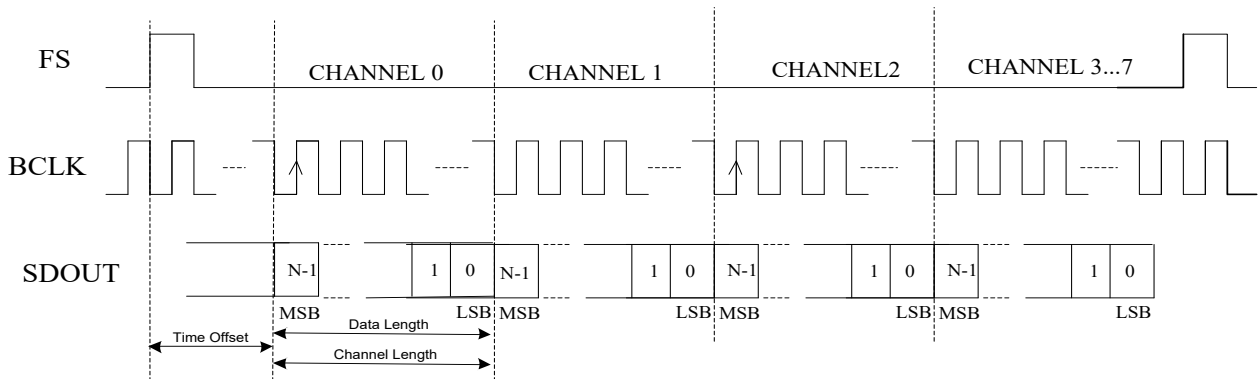


Figure 33 PCM Time Offset Audio Data

6.15.6 TDM/PCM Interface Timing

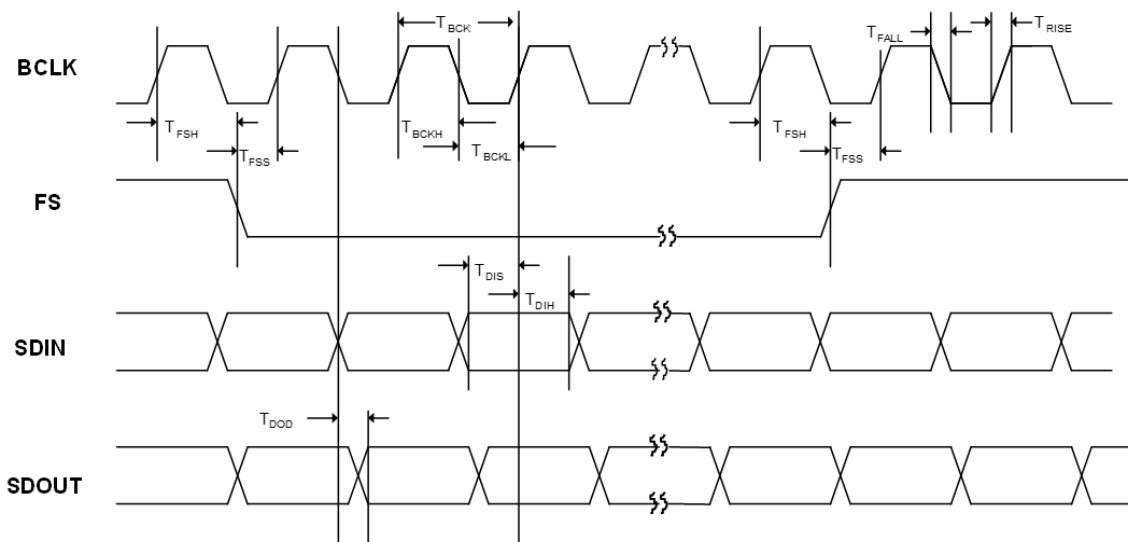


Figure 34 TDM/PCM Interface Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T _{BCK}	BCLK Cycle Time in Slave Mode	40	-	-	ns
T _{BCKH}	BCLK High Pulse Width in Slave Mode	17	-	-	ns
T _{BCKL}	BCLK Low Pulse Width in Slave Mode	17	-	-	ns
T _{FSS}	FS to BCLK Rising Edge Setup Time in Slave Mode	15	-	-	ns
T _{FSH}	BCLK Rising Edge to FS Hold Time in Slave Mode	15	-	-	ns
T _{RISE}	Rise Time for All Audio Interface Signals	-	-	0.135T _{BCK}	ns
T _{FALL}	Fall Time for All Audio Interface Signals	-	-	0.135T _{BCK}	ns
T _{DIS}	SDIN to BCLK Rising Edge Setup Time	10		-	ns
T _{DIH}	BCLK Rising Edge to SDIN Hold Time	10		-	ns
T _{DOD}	BCLK Falling Edge to ADCOUT Delay Time	-	-	10	ns

Table 38 TDM/PCM Interface Parameters

6.16 Interrupt Request

Interrupt Request is a useful error checking feature that can indicate problems on the amplifier during use. Below is the registers used to control the nature of the request. Please refer to the corresponding register for more information.

Register Name	Address	Description / Range
INT_dis_WDT	0x05[14]	0 = Enabled 1 = Disabled
INT_dis_OTP	0x05[12]	0 = Enabled 1 = Disable
INT_dis_OVLO	0x05[11]	0 = Enabled 1 = Disabled
INT_dis_UVLO	0x05[10]	0 = Enabled 1 = Disabled
INT_dis_SCP	0x05[9]	0 = Enabled 1 = Disabled
INT_dis_audclk_det	0x05[8]	0 = Enabled 1 = Disabled
INT_msk_WDT	0x05[6]	0 = Enable INT 1 = Mask INT
INT_msk_OTP	0x05[4]	0 = Enable INT 1 = Mask INT
INT_msk_OVLO	0x05[3]	0 = Enable INT 1 = Mask INT
INT_msk_UVLO	0x05[2]	0 = Enable INT 1 = Mask INT
INT_msk_SCP	0x05[1]	0 = Enable INT 1 = Mask INT
INT_msk_audclk_det	0x05[0]	0 = Enable INT 1 = Mask INT
INT_WDTR_status	0x06[8]	0 = Normal 1 = WDT-Rch abnormal
INT_WDTL_status	0x06[6]	0 = Normal 1 = WDT-Lch abnormal
INT_OTP_statusc	0x06[4]	0 = Normal 1 = over temperature
INT_OVLO_status	0x06[3]	0 = Normal 1 = over voltage lock out
INT_UVLO_status	0x06[2]	0 = Normal 1 = under voltage lock out

Register Name	Address	Description / Range
INT_SCP_status	0x06[1]	0 = Normal 1 = Short current protection
INT_audclk_det_status	0x06[0]	0 = Normal 1 = Audio Clock Detection abnormal
IRQ_PL	0x0A[15]	Polarity of IRQZ 0 = Active Low 1 = Active High
IRQ_EN	0x0A[11]	IRQZ enable 0 = Disable the IRQZ output 1 = Output IRQZ

Table 39 Interrupt Registers

A brief overview of the feature is that the physical IRQZ pin [30] goes to active logic when one of the bits in **0x06[8:0].INT_CLR_STATUS** become activated when IRQ function is enabled by setting **0x0A[11].IRQ_EN**. The polarity to indicate Interrupt can be configured in **0x0A[15].IRQ_PL**.

Assuming that it is using active high logic (meaning the register will become one when triggered) set **0x0A[15].IRQ_PL = 1'b1**. Additionally, this IRQZ pin [30] should be connected to the external interrupt of its controller, of which the controller will activate its Interrupt Service Routine (ISR) when IRQZ pin goes high. The ISR should then read **0x06[8:0].INT_CLR_STATUS** register, reset the same register by sending a single bit 1 to the activated bit in that register, and trigger a flag to fix what may have happened depending on the interrupt status shown in **0x06[8:0].INT_CLR_STATUS**. NOTE: Only one bit can be reset at a time.

What shows in the IRQZ pin [30] and the status register is controlled by the **0x05[15:0].INTERRUPT_CTRL** register. The top bits [15:8] control whether the conditions would show up in both the **0x06[8:0].INT_CLR_STATUS** register and IRQZ pin while the lower bits (mask) [7:0] will let it show on the **0x06[8:0].INT_CLR_STATUS** register but not on the IRQZ pin. In short, the IRQZ pin is latched to all of the triggering bits in the **0x06[8:0].INT_CLR_STATUS** register and will go low when all bits in the **0x06[8:0].INT_CLR_STATUS** register is reset.

An example of this is when Over Voltage Lock Out (OVLO) occurs during activation of output. On initial register loading, we set **0x0A[15].IRQ_PL = 1'b1** and **0x0A[11].IRQ_EN = 1'b1** meaning IRQ logic is active high and output is enable. Additionally we want to set the **0x05[15:0].INTERRUPT_CTRL** to 0x01 which enables the Watch dog timer, current/temperature protection, low/over voltage protection, and Audio Clock Detection but masks the interrupt detecting Audio Clock.

6.17 Advanced DSP Core

NAU83G60 consist of two Advanced DSP core. Each channel is equipped with an Advanced DSP core. DSP Core Clock should be provided up to 122.88MHz (48KHz sample rate base) or 112.896MHz (44.1KHz sample rate base) by an on-chip MCLK PLL. The NAU83G60 DSP Core runs Klippel's Non-Linear Speaker Protection Algorithm: Klippel Controlled Sound (KCS). In Advanced DSP processing, the Audio sample rate is 48KHz or 44.1KHz.

6.17.1 Reset and Clocks

NAU83G60 Advanced DSP Core is released from reset after either a Hardware reset or a Software reset. Whenever the Advanced DSP is reset, the protection algorithm will be reinitialized, and the host processor should re-communicate with the KCS library and reinstate speaker parameters.

NAU83G60 DSP Core Clock is derived from the provided MCLK, HIRC48MHz or PLL. Refer to Figure 13. Configure DSP Core Clock frequency to 122.88MHz (48KHz sample rate base) or 112.896MHz (44.1KHz sample rate base).

6.17.2 DSP Core Control

The DSP core control interface allows I2C communication between the DSP running KCS algorithm and the outside world (i.e. Host processor). A communication protocol is implemented through I2C to provide different the ability to load speaker configurations, called Klippel Controlled Sound (KCS) Setups. These speaker configurations are fine-tuned to the speakers that the device will be outputting and utilizes Klippel™ non-linear control algorithm to maximize volume and frequency without causing any harm to the speaker.

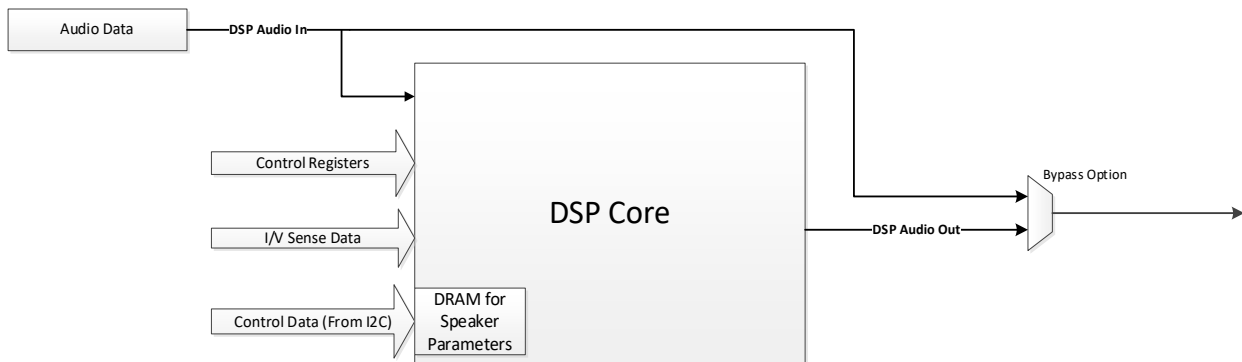


Figure 35 Advanced DSP Connection Diagram

A typical setup would be to initialize through register settings and introduce a KCS setup unique to the speaker used. This KCS setup uses an I2C communication protocol.

The communication register **REG0xF000** is used as the main channel to communicate directly to the DSP left core. Likewise, the communication register for DSP right core is **REG0xF002**. That can request status information, get or set the current speaker parameters, or get speaker diagnostic data. This is a special register which has a two byte address and will return with four bytes of data. When read without invoking a command, this register will either return all zeros, **0x000000** in byte segments, or an idle word **0xF4F3F2F1** in byte segments.

The steps will ensure that the DSP is initialized. First, **MCLK**, **BCLK**, and **Frame Sync**, as part of the I2S Signal input, must be provided before the chip is fully initialized. Second, the DSP needs to be stalled during the initialization by setting **0x1A[4].DSP_RUNSTALL** as 1. Third, after loading the register

settings the chip must go through a soft-reset. This is done by writing **0x5A5A** then **0xA5A5** to **0x01[15:0].RESET_N_SOFT_PRE**. The DSP then shall be released by setting **0x1A[4].DSP_RUNSTALL** as 0 to un-stall, and **0x12[5].SEL_DSP_DAC** as 1 to select DSP output.

To verify a correct setup, the register **0xF000** or **0xF002** can be read and is the main line of communication to the DSP through the I2C communication protocol. After setting the correct register settings, the NAU83G60 will return the four bytes idle word, **0xF4F3F2F1**.

Register Name	Address	Description / Range
RESET_N_SOFT_PRE	0x01[15:0]	Write this register twice to reset all internal stated machines without resetting the registers. Write 0x5A5A -> 0xA5A5 0x5A5A = Enable the internal SW reset. 0xA5A5 = Release the internal SW reset.
DSP_RUNSTALL	0x1A[4]	Stall the Advanced DSP core 1 = Stall Advanced DSP 0 = Run Advanced DSP
SEL_DSP_DAC	0x12[5]	0 = Bypass DSP path 1 = DSP path

Table 40 DSP Core Control Registers

6.18 Initialization

6.18.1 Host Processor POR Procedure

At power up Host Processor is expected to set initial configuration of NAU83G60, and then configure the KCS protection algorithm. NAU83G60 DAC and ADC sampling rate must be set before the DSP initialization sequence.

In order to properly configure DSP, MCLK and DSP_CLK must be provided and set to a correct frequency. Host Processor then configures NAU83G60 for the required sampling rate of both the audio input and sensor data. This configuration sequence can be part of the normal NAU83G60 initialization sequence that includes all the subsystems (filters, ALC, etc.). Once CODEC configuration is done, Host processor issues a Soft Reset. DSP is then re-initialized according to the flow provided separately by Nuvoton to load KCS configuration parameters.

6.18.2 Power On Initialization

After power up NAU83G60, Host need to initialize NAU83G60 to build up internal power, clock and audio digital interface. Below steps shows only as an example. For real applications, please refer to SW driver provided by Nuvoton.

Register	Value	//Explanation
// initial phase		
0000	5A5A	// Reset Chip
0000	A5A5	// Reset Chip
0078	0000	// Enable Digital LDO
0077	0000	// Enable Software Shutdown Mode
009D	0003	// Stall HW1 PEQ Engine and Clear DRAM to Zero
009D	0001	// Stall HW1 PEQ Engine
007E	A5A5	// Enable Clock Gate
0002	0001	// Latch I2C LSB Value
000F	0000	// Clear Slot Assignment from V _{BAT} and PDM Right Channel
0010	3114	// Set ANC Left Channel as Slot 1 and Right Channel as Slot 3
0010	3100	// Clear Slot Assignment from TEMP Right Channel
0017	0000	// Clear Slot Assignment from AEC Right Channel
000B	0102	// Clear Reserved Bit and set I2S format
0071	0212	// Set DAC Clock Divider as 2 and Chopper Divider as 16
005D	0011	// Set DAC SINC OSR as 32 and IVSENSE BS OSR as 32
006E	0E95	// DAC gain setting 0dB by changing current cell current
005F	F407	// Set Trim Bit Control of DLDO and GVDD to The Highest Voltage
0040	0A00	// Disable Data and Clock Detection Settings, include FS_MCLK_DET and FS_BCLK_DET
008C	0005	// Set HW3 Droop and Filter Sample as 192K
009C	19FF	// Set HW1 Mute, Mute Interval as 699ms and HW1 Zero THD as 0xFF

```

0096    000D    // Set HW2 Droop with 192K and normal latency
0096    800D    // Enable HW1 ANC
0097    BF66    // Set HW2 Left Default Volume
0098    BF66    // Set HW2 Rigjt Default Volume
0099    01FF    // Set HW2 Mute and Threshold of Zero Crossing
0012    06F0    // Set Default Audio Stream Path HW1->DSP->HW2->SINC->HW3
0007    0000    // Set Input Status as Low and Input/Output Mode Disable for All GPIO
0008    8181    // Set GPIO1 and GPIO2 MUX as Reserved
0009    1E9E    // Set GPIO3 MUX as Clock output
0080    0A84    // Enable Clock output with TCK_DIV as 3 from PLL source
006A    DC4B    // Enable SARADC with Extra Average Filter of VBAT and Select CH1 Temperature
006B    C60F    // Enable Temperature Sensor, VBATDIV and VRF. Set Average Filter Data as 16
for VTEMP and VBAT.
006C    F000    // Enable IV sense internal LDO
006D    0F5C    // Enable Bias Current and Reference Voltage for IVSENSE. Set VSNS Gain as
1/12 and ISNS Gain as x16(24dB). Set PGA Current as 2'b11 and SDN Delay as 2'b00.
00A4    7FA8    // The sawtooth clock from ivsense clock, PWM frequency 432 Khz
00A5    27EE    // Configure sawtooth PLL APR
0068    0060    // Config trim short current reference. Enable Non-overlap longer delay. Set
segment driver as half driving strength.
0067    8170    // Enable SCP Clear Mode and Class D Modulator to Common Mode
0067    8190    // Set Analog Mute and Class D Modulator Gain as 14dB
008A    BE90    // Adjust HW3 Default Left Volume of Voltage Sense
008B    BE90    // Adjust HW3 Default Right Volume of Voltage Sense
008D    C24C    // Adjust HW3 Default Left Volume of Current Sense
008E    C24C    // Adjust HW3 Default Right Volume of Current Sense
008F    00FF    // Set HW3 Zero THD as 0xFF
000D    02C0    // Enable TX SDOUT and Data at BCLK Rising. Enable Left Voltage Sense at Slot
0 and Set Slot length as 16 bit.
000E    C400    // Enable Left Current Sense at Slot 1 and Set Slot length as 16 bit. Clear Slot
Assignment from Left Channel PDM.
0011    C8CC    // Enable Right Voltage Sense at Slot 2 and Set Slot length as 16 bit. Enable Right
Current Sense at Slot 3 and Set Slot length as 16 bit.
007A    7D00    // Set DAC Channel Temperature Trim Code Slope as 0x7D
007B    1A00    // Set ISense temperature trim code slope as 0x1a
007C    67F0    // Set misc trim config as 0x67F0
0060    0018    // Enable Efuse Initianllization
0090    6000    // Clear HW2 DRAM

```

```

0090    2000    // Finish HW2 DRAM Clear
0086    6000    // Clear HW3 DRAM
0086    2000    // Finish HW3 DRAM Clear
// switch to internal clock for kcs loading
0072    CC44    // Enable PLL power
0072    CF44    // Select HIRM48 as PLL source
0073    0701    // Expect for PLL output is 12.5MHz, so pll_div(MSEL): 8, pll_int(NSEL):2,
0074    0155    // pll_frac(XSEL): 341
0040    0880    // Set SRATE=48KHz and MCLK_RATE=12.288MHz
0072    8344    // Set PLLOUT_DIV = 0
0003    0040    // Set DSP_CLK_SEL from PLL
0004    8800
0071    0112    // Enable clock for analog clock for DAC and IVSense ADC
0001    5A5A    // Software Reset
0001    A5A5    // Software Reset
// Set Left and Right PEQ parameter, respectively, or current default audio stream path will have noise.
009D    0005    // Stall HW1 PEQ Engine. Enable coefficient writing.
0101    0020    // Left PEQ
010d    0020
0119    0020
0125    0020
0131    0020
013D    0020
0149    0020
0155    0020
0161    0020
016D    0020
0179    0020
0185    0020
0191    0020
019D    0020
01A9    0020
0201    0020    // Right PEQ
020D    0020
0219    0020
0225    0020

```

```

0231    0020
023D    0020
0249    0020
0255    0020
0261    0020
026D    0020
0279    0020
0285    0020
0291    0020
029D    0020
02A9    0020
009D    0001    // Disable coefficient writing
0090    0000    // Uninstall HW2 Engine
009D    0000    // Uninstall HW1 Engine
#if DSP enable
0086    0000    // Uninstall HW3 Engine
001A    0000    // Uninstall DSP

// DSP initializing, loading KCS firmware ...//

009D    C000    // PEQ Band numbers control for DSP
#else DSP bypass
009D    8000    // PEQ Band numbers control when bypassing DSP
#endif
00A5    13EE    // Config sawtooth clock for VBAT 12V. Class D modulator input short setting for
mute and de-pop
// purpose. Restore normal after initiation.

```

Register Name	Address	Description / Range
SW_SD	0x77[15:0]	Software Shut down mode of whole chip write 55AA to shut down (disable) write others to enable
PD_SW_DLDO	0x78[15:0]	Software Power down of 1.5V digital LDO Write AA55 to power down (disable) Write others to enable

Table 41 Power on Initialization Registers

6.19 Device Register Table

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	HWWARE_RST	RESET_N1																Register Reset Write this register twice to reset all the registers. Write 0x5A5A -> 0x5A5A 0x5A5A = Enable the internal SW reset. 0x5A5A = Release the internal SW reset.	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	DSP_SOFTWARE_RST	RESET_N_SOFT_PRE																Software Reset Write 0x5A5A -> 0x5A5A to reset all internal stated machines without resetting the registers. 0x5A5A = Enable the internal SW reset. 0x5A5A = Release the internal SW reset.	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
2	I2C_ADDR_LATCH	I2C_ADDR_LCH																I2C Address Latch Write 1 to latch I2C Device address	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W	

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
3	CLK_CTL0	MCLK_DIV																MCLK Divider Select MCLK divider = MCLK_DIV + 1 000000 = 1 (DEFAULT)	
		DSP_CLK_DIV																DSP Clock Divider Select DSP_CLK divider = DSP_CLK_DIV + 1 000 = 1 (DEFAULT)	
		DSP_CLK_SEL																DSP Clock Select 00 = MCLK (DEFAULT) 01 = HIRC48M 10 = PLL 11 = RESERVED	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
4	CLK_CTL1	MCLK_SEL																	MCLK Select 00 = MCLK (DEFAULT) 01 = HIRC48M 10 = PLL 11 = RESERVED
		HW_CLK_SEL																	HW Engine Clock Select 00 = MCLK (DEFAULT) 01 = HIRC48M 10 = PLL 11 = RESERVED
		HW_CLK_DIV																	HW Clock Divider Select HW_CLK divider = HW_CLK_DIV + 1 000 = 1 (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
5	INTERRUPT_CTRL	INT_dis_WDT																	WatchDog Interrupt Disable Control 0 = Enable 1 = Disable (DEFAULT)
		INT_dis_OTP																	OTP Interrupt Disable Control 0 = Enable (DEFAULT) 1 = Disable
		INT_dis_OVLO																	OVLO Interrupt Disable Control 0 = Enable (DEFAULT) 1 = Disable
		INT_dis_UVLO																	UVLO Interrupt Disable Control 0 = Enable (DEFAULT) 1 = Disable
		INT_dis_SCP																	SCP Interrupt Disable Control 0 = Enable (DEFAULT) 1 = Disable
		INT_dis_audclk_det																	Audio Clock Detection Interrupt Disable Control 0 = Enable (DEFAULT) 1 = Disable
		INT_msk_WDT																	WatchDog Interrupt Mask Enable Control 0 = Disable 1 = Enable (DEFAULT)
		INT_msk_OTP																	OTP Interrupt Mask Control 0 = Disable 1 = Enable (DEFAULT)
		INT_msk_OVLO																	OVLO Interrupt Mask Control 0 = Disable 1 = Enable (DEFAULT)
		INT_msk_UVLO																	UVLO Interrupt Mask Control 0 = Disable 1 = Enable (DEFAULT)
		INT_msk_SCP																	SCP Interrupt Mask Control 0 = Disable 1 = Enable (DEFAULT)
		INT_msk_audclk_det																	Audio Clock Detection Interrupt Mask Control 0 = Disable 1 = Enable (DEFAULT)
		DEFAULT	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0x40FF – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6	INT_CLR_STATUS	INT_flag_WDTR																	Right Channel WatchDog Interrupt Flag Select (Write 1 to clear) 0 = Normal (DEFAULT) 1 = WDT-Rch
		INT_flag_WDTL																	Left Channel WatchDog Interrupt Flag Select (Write 1 to clear) 0 = Normal (DEFAULT) 1 = WDT-Lch
		INT_flag_OTP																	OTP Interrupt Flag Select (Write 1 to clear) 0 = Normal (DEFAULT) 1 = Abnormal over temperature
		INT_flag_OVLO																	OVLP Interrupt Flag Select (Write 1 to clear) 0 = Normal (DEFAULT) 1 = Abnormal over voltage Lock
		INT_flag_UVLO																	UVLO Interrupt Flag Select (Write 1 to clear) 0 = Normal (DEFAULT) 1 = Abnormal under voltage lock out
		INT_flag_SCP																	SCP Interrupt Flag Select (Write 1 to clear) 0 = Normal (DEFAULT) 1 = Abnormal Short current protection
		INT_flag_audclk_det																	Audio Clock Detection Interrupt Flag Select (Write 1 to clear) 0 = Normal (DEFAULT) 1 = Abnormal detection
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
7	GP_CTRL	GPIO1_IEOE																	GPIO1 Mode Select 00 = Input / output disable 01 = Output Enable 10 = Input Enable (DEFAULT) 11 = NOT allowed
		GPIO2_IEOE																	GPIO2 Mode Select 00 = Input / output disable 01 = Output Enable 10 = Input Enable (DEFAULT) 11 = NOT allowed
		GPIO3_IEOE																	GPIO3 Mode Select 00 = Disable input / output 01 = Output Enable 10 = Input Enable (DEFAULT) 11 = NOT allowed
		GPIO4_IEOE																	GPIO4 Mode Select 00 = Input / output disable 01 = Output Enable 10 = Input Enable (DEFAULT) 11 = NOT allowed
		GPIO1_Input_Status																	GPIO1 Input Status (RO) 0 = Low 1 = High
		GPIO2_Input_Status																	GPIO2 Input Status (RO) 0 = Low 1 = High
		GPIO3_Input_Status																	GPIO3 Input Status (RO) 0 = Low 1 = High
		GPIO4_Input_Status																	GPIO4 Input Status (RO) 0 = Low 1 = High
		DEFAULT	1	0	1	0	1	0	1	0	x	x	x	x	0	0	0	0	0xAAX0 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8	GP_CTL0	GPIO2_MUX																	GPIO2 MUX Select 00 = GPIO2 (DEFAULT) 01 = RESERVED 10 = RESERVED 11 = RESERVED
		GPIO2_SR																	GPIO2 Slew Rate Select 0 = Fast (DEFAULT) 1 = Slow
		GPIO2_CDS																	GPIO2 Current Drive Select 00 = Low 01 = High 10 = Large 11 = Max (DEFAULT)
		GPIO2_PS																	GPIO2 Pull Select 0 = Pull Down 1 = Pull Up (DEFAULT)
		GPIO2_PE																	GPIO2 Pin Pull Enable Control 0 = Disable 1 = Enable (DEFAULT)
		GPIO1_MUX																	GPIO1 MUX Select 00 = GPIO1 (DEFAULT) Others = RESERVED
		GPIO1_SR																	GPIO1 Slew Rate Select 0 = Fast (DEFAULT) 1 = Slow
		GPIO1_CDS																	GPIO1 Current Drive Select 00 = Low 10 = Large 01 = High 11 = Max (DEFAULT)
		GPIO1_PS																	GPIO1 Pull Select 0 = Pull Down 1 = Pull Up (DEFAULT)
		GPIO1_PE																	GPIO1 Pin Pull Enable Control 0 = Disable 1 = Enable (DEFAULT)
		DEFAULT	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0x1E1E – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
9	GP_CTL1	GPIO4_MUX																	GPIO4 MUX Select 00 = GPIO4 (DEFAULT) 01 = RESERVED 10 = Test_clk out 11 = RESERVED
		GPIO4_SR																	GPIO4 Slew Rate Select 0 = Fast (DEFAULT) 1 = Slow
		GPIO4_CDS																	GPIO4 Current Drive Select 00 = Low 01 = High 10 = Large 11 = Max (DEFAULT)
		GPIO4_PS																	GPIO4 Pull Select 0 = Pull Down 1 = Pull Up (DEFAULT)
		GPIO4_PE																	GPIO4 Pin Pull Enable Control 0 = Disable 1 = Enable (DEFAULT)
		GPIO3_MUX																	GPIO3 MUX Select 00 = GPIO3 (DEFAULT) 01 = RESERVED 10 = Test_clk out 11 = RESERVED
		GPIO3_SR																	GPIO3 Slew Rate 0 = Fast (DEFAULT) 1 = Slow
		GPIO3_CDS																	GPIO3 Current Drive Select 00 = Low 01 = High 10 = Large 11 = Max (DEFAULT)
		GPIO3_PS																	GPIO3 Pull Select 0 = Pull Down 1 = Pull Up (DEFAULT)
		GPIO3_PE																	GPIO3 Pin Pull Enable Control 0 = Disable 1 = Enable (DEFAULT)
		DEFAULT	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0x1E1E – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
A	GP_CTL2	IRQ_PL																	IRQZ Output Pin Polarity to Indicate Interrupt Select 0 = Active Low (DEFAULT) 1 = Active High
		IRQ_EN																	IRQZ Enable Control 0 = Disable (DEFAULT) 1 = Enable
		GPIO4_CS																	GPIO4 Input Type Select 0 = CMOS Buffer (DEFAULT) 1 = Schmitt Trigger
		GPIO3_CS																	GPIO3 Input Type Select 0 = CMOS Buffer (DEFAULT) 1 = Schmitt Trigger
		GPIO2_CS																	GPIO2 Input Type Select 0 = CMOS Buffer (DEFAULT) 1 = Schmitt Trigger
		GPIO1_CS																	GPIO1 Input Type Select 0 = CMOS Buffer (DEFAULT) 1 = Schmitt Trigger
		GPIO4OUT																	GPIO4 Programmable Output Select 0 = Low (DEFAULT) 1 = High
		GPIO3OUT																	GPIO3 Programmable Output Select 0 = Low (DEFAULT) 1 = High
		GPIO2OUT																	GPIO2 Programmable Output Select 0 = Low (DEFAULT) 1 = High
		GPIO1OUT																	GPIO1 Programmable Output Select 0 = Low (DEFAULT) 1 = High
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
B	I2S0_PC M_CTRL1	EN_TDM_TX																	TDM TX Enable Control 0 = Disable (DEFAULT) 1 = Enable
		EN_TDM_RX																	Enable TDM RX 0 = Disable (DEFAULT) 1 = Enable
		FRAME_START																	TDM Frame Start Polarity 0 = Frame start while Low to High edge on FS 1 = Frame start while High to Low edge on FS (DEFAULT)
		RX_JUSTIFY																	TDM RX Sample Justification Within the Time Slot Select 0 = Left (DEFAULT) 1 = Right
		RX_OFFSET																	RX Offset Select (BCLK cycles in between FS transition start to slot0.) 00000 = I2S Left / Right Justify (DEFAULT) 00001 = I2S_Normal/TDDM_I2S Others = Based on user requirement on TDM
		DEFAULT	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	0	0x0702 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
C	I2S0_PC_M_CTRL2	TDM_SDO_PU																	TDM SDO Pull Up Enable Control 0 = Disable (DEFAULT) 1 = Enable
		TDM_SDO_PD																	TDM SDO Pull Down Select 0 = Floating (DEFAULT) 1 = Internal Pull-down TDM SDO
		TDM_DLEN																	Data Length of TDM Select 00 = 16 bits 01 = 20 bits 10 = 24 bits (DEFAULT) 11 = 32 bits
		TDM_CLEN																	Channel Length of TDM Select 00 = 16 bits 01 = 24 bits 10 = 32 bits (DEFAULT) 11 = RESERVED
		RX_Audio_R																	TDM RX Audio Right Channel Time Slot Selection, Unit in Byte
		RX_Audio_L																	TDM RX Audio Left Channel Time Slot Selection, Unit in Byte
		DEFAULT	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0x0A10 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
D	I2S0_PC_M_CTRL3	TX_LSB_CFG																	TDM TX SDOUT LSB Data Select 0 = TDM TX SDOUT LSB is driven for full cycle (DEFAULT) 1 = TDM TX SDOUT LSB is driven for half cycle
		TX_FILL																	TX_FILL, Unused TX SDOUT Bit Field Filling Select 0 = Transmitted 0 1 = Hi-Z (DEFAULT)
		TX_OFFSET																	TX_Offset: BCLK cycles in between FS start and first TX slot0 In general, it is “1” for I2S and “0” for left justify
		VSNS_L_SL_EN																	TDM TX VSNS Left Channel Slot Length Select 0 = 8-bit (DEFAULT) 1 = 16-bit
		VSNS_L_TX_EN																	Transmission of V_{sense} Left Channel Data Enable Control 0 = Disable (DEFAULT) 1 = Enable
		VSNS_L_SLOT																	TDM TX Voltage sense Left channel time slot, Unit in byte
		DEFAULT	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0x1300 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
E	I2S0_DATA_CTRL1	ISNS_L_SL_EN																	TDM TX I_{sense} Left Channel Slot Length Select 0 = 8-bit (DEFAULT) 1 = 16-bit
		ISNS_L_TX_EN																	Transmission Of I_{sense} Left Channel Data Select 0 = Disable (DEFAULT) 1 = Enable
		ISNS_L_SLOT																	TDM TX Current sense Left channel time slot, Unit in byte
		PDM_L_SL_EN																	PDM Left Channel Sample Slot Length of TDM TX Select 0 = 16-bit (DEFAULT) 1 = 32-bit
		PDM_L_TX_EN																	PDM Left Channel Data to TDM TX Transmit Enable Control 0 = Disable (DEFAULT) 1 = Enable
		PDM_L_SLOT																	PDM left channel time slot of TDM TX, Unit in byte
		DEFAULT	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0x0304 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
F	I2S0_DATA_CTRL2	VBAT_TX_EN																	VBAT Transmit to TDM TX Enable Control 0 = Disable (DEFAULT) 1 = Enable
		VBAT_SLOT																	VBAT Time Slot of TDM TX, Unit in Byte
		PDM_R_SL_EN																	PDM Right Channel Sample Slot Length of TDM TX Select 0 = 16-bit (DEFAULT) 1 = 32-bit
		PDM_R_TX_EN																	PDM Right Channel Data to TDM TX Enable Control 0 = Disable (DEFAULT) 1 = Enable
		PDM_R_SLOT																	PDM Right Channel Time Slot of TDM TX, Unit in Byte
		DEFAULT	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0x080B – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
10	I2S0_DATA_CTRL3	RX_ANC_R																	ANC Right Channel Time Slot of TDM RX, Unit in Byte
		RX_ANC_L																	ANC Left Channel Time Slot of TDM RX, Unit in Byte
		TDM_LOOPBACK																	TDM Interface Loopback Enable Control (SDO = SDI) 0 = Disable (DEFAULT) 1 = Enable
		TJ_TX_EN																	Tj Transmit to TDM TX Enable Control 0 = Disable (DEFAULT) 1 = Enable
		TJ_SLOT																	Tj Time Slot of TDM TX, Unit in Byte
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0x0014 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
11	I2S0_DATA_CTRL4	VSNS_R_SL_EN																	TDM TX V _{Sense} Right Channel Slot Length Select 0 = 8-bit (DEFAULT) 1 = 16-bit
		VSNS_R_TX_EN																	Transmission Of V _{Sense} Right Channel Data Enable Control 0 = Disable (DEFAULT) 1 = Enable
		VSNS_R_SL_OT																	TDM TX Voltage Sense Right Channel Time Slot, Unit in Byte
		ISNS_R_SL_EN																	TDM TX I _{Sense} Right Channel Slot Length Select 0 = 8-bit (DEFAULT) 1 = 16-bit
		ISNS_R_TX_EN																	Transmission Of I _{Sense} Right Channel Data Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ISNS_R_SL_OT																	TDM TX Current Sense Right Channel Time Slot, Unit in Byte
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0x0014 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
12	PATH_CTRL	SEL_HW1																	HW1 Output Select 0 = HW1 bypass 1 = HW1 output (DEFAULT)
		AUDIO_SINC_SEL																	SINC Filter Select 0 = Bypass SINC filter (DEFAULT) 1 = SINC filter path
		SEL_HW2																	HW2 Output Select 0 = HW2 bypass (DEFAULT) 1 = HW2 path
		SEL_DSP_DAC																	DSP DAC Select 0 = Bypass DSP (DEFAULT) 1 = DSP path
		SEL_HW3																	HW3 Output Select 0 = HW3 bypass (DEFAULT) 1 = HW3 path
		DEFAULT	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0x0400 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
17	I2S0_DATA_CTRL5	AEC_L_TX_SLEN																	TDM TX AEC L-CH Slot Length Select 0 = 16-bit (DEFAULT) 1 = 32-bit
		AEC_L_TX_EN																	TDM TX AEC L-CH Enable Control 0 = Disable (DEFAULT) 1 = Enable
		AEC_L_TX_SLOT																	TDM TX AEC L-CH Slot Assignment
		AEC_R_TX_SLEN																	TDM TX AEC R-CH Slot Length Select 0 = 16-bit (DEFAULT) 1 = 32-bit
		AEC_R_TX_EN																	TDM TX AEC R-CH Enable Control 0 = Disable (DEFAULT) 1 = Enable
		AEC_R_TX_SLOT																	TDM TX AEC R-CH slot assignment, Unit in byte
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0x0014 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1A	DSP_CORE_CTRL2	DSP_RUNSTALL																	Stall The Advanced DSP Core 0 = Run Advanced DSP 1 = Stall Advanced DSP (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x0010 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
21	VBAT_READOUT	VBAT_READOUT																	VBAT_OUT[11:0] (RO)
		DEFAULT	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0x0XXX – R

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
22	TEMP_READOUT	TEMP_READOUT																	TEMP_OUT[11:0] (RO)
		DEFAULT	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0x0XXX – R

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
2C	ALC_CTRL1	ALCMAXGAIN																	Maximum ALC Gain Select 000 = RESERVE (DEFAULT) 111 = 0 dB Other = Reserve
		ALCMINGAIN																	Minimum ALC Gain Setting 000 = -3 dB (DEFAULT) 001 = -6 dB 010 = -9 dB 011 = -12 dB 100 = -16 dB 101 ~ 111 = RESERVED
		DEFAULT	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0x2000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
2D	ALC_CTRL2	ALCDCY																	Interval of Peak Level Detection in ALC Release State Select 0000 = 0.5 ms/step 0001 = 1 ms/step 0010 = 2 ms/step 0011 = 4 ms/step 0100 = 8 ms/step 0101 = 16 ms/step 0110 = 32 ms/step 0111 = 64 ms/step 1000 = 128 ms/step (DEFAULT) 1001 = 256 ms/step 1010 = 512 ms/step 1011 = 1024ms/step 1100 ~ 1111 = RESERVED
		ALCATK																	ALC Attack Timer (0.25dB/ adjust step) Decrease Select 0000 = 2 μs/step 0001 = 4 μs/step 0010 = 8 μs/step 0011 = 16 μs/step 0100 = 32 μs/step (DEFAULT) 0101 = 64 μs/step 0110 = 128 μs/step 0111 = 256 μs/step 1000 = 512 μs/step 1001 = 1024 μs/step 1010 = 2048 μs/step 1011 = 4096 μs/step 1100 ~ 1111 = RESERVED
		ALCHLD																	Hold Time Before ALC Automated Gain Increase Select 0000 = 0.00 ms (DEFAULT) 0001 = 2.00 ms 0010 = 4.00 ms 0011 = 8.00 ms 0100 = 16.00 ms 0101 = 32.00 ms 0110 = 64.00 ms 0111 = 128.00 ms 1000 = 256.00 ms 1011 = 512.00 ms 1010 ~ 1111 = 1024ms
		ALCLVL																	ALC Target Level Select (The Limiter Level Of ALC, step size is -1dB.)0000 = 0 dBFS (DEFAULT) 0001 = -1 dBFS 0010 = -2 dBFS ▼ 1110 = -14 dBFS 1111 = -15 dBFS
		DEFAULT	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0x8400 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
2E	ALC_CTRL3	ALCUVLOP_EN																	ALC / UVLOP Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0x2083 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
31	UVLOP_CTRL1	UVLOP_EN																	UVLOP Enable Control 0 = UVLOP disable (fixed gain) (DEFAULT) 1 = UVLOP enable
		UVLOP_MAX_GAIN																	Maximum UVLOP Gain Select 111 = 0 dB 000 = RESERVE (DEFAULT) Other = RESERVED
		UVLOP_MIN_GAIN																	Minimum UVLOP Gain Select 000 = -3 dB (DEFAULT) 001 = -6 dB 010 = -9 dB 011 = -12 dB 100 = -16 dB 101 ~ 111 = RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
32	UVLOP_CTRL2	UVLOPDCY																	UVLOP Decay Timer (0.25dB/ Adjust Step) 0000 = 0.5 ms/step 0001 = 1 ms/step 0010 = 2 ms/step 0011 = 4 ms/step 0100 = 8 ms/step 0101 = 16 ms/step 0110 = 32 ms/step 0111 = 64 ms/step 1000 = 128 ms/step (DEFAULT) 1001 = 256 ms/step 1010 = 512 ms/step 1011 = 1024ms/step 1100 ~ 1111 = RESERVED
		UVLOPATK																	UVLOP Attack Timer (0.25dB/ Adjust Step) 0000 = 2 μs/step 0001 = 4 μs/step 0010 = 8 μs/step 0011 = 16 μs/step 0100 = 32 μs/step (DEFAULT) 0101 = 64 μs/step 0110 = 128 μs/step 0111 = 256 μs/step 1000 = 512 μs/step 1001 = 1024 μs/step 1010 = 2048 μs/step 1011 = 4096 μs/step 1100 ~ 1111 = RESERVED
		UVLOPHLD																	Hold Time Before UVLOP Automated Gain Increase 0000 = 0.00 ms (DEFAULT) 0001 = 2.00 ms 0010 = 4.00 ms 0011 = 8.00 ms 0100 = 16.00 ms 0101 = 32.00 ms 0110 = 64.00 ms 0111 = 128.00 ms 1000 = 256.00 ms 1011 = 512.00 ms 1010 ~ 1111 = 1024ms
		UVLOPLVL																	UVLOP Target Level Select (The limiter level of UVLOP, step size is -1dB.) 0000 = 0 dBFS (DEFAULT) 0001 = -1 dBFS 0010 = -2 dBFS ▼ 1110 = -14 dBFS 1111 = -15 dBFS UVLOPLVL should be lower than ALCLVL
		DEFAULT	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0x8400 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
33	UVLOP_CTRL3	UVLOP_VBAT_HYST																	V _{BAT} Hysteresis Voltage of UVLOP Dec2Hex [Round(123.53 * UVLOP_VBAT_HYST)]
		UVLOP_DETECT_RATE																	UVLOP Audio Signal Detect RATE Select 00 = Default (DEFAULT) 01 = RESERVED 10 = RESERVED 11 = Fast
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
40	CLK_DET1	APWRUPEN																	Data Non-Zero Counter Enable Control (The audio clock detection will require non_zero samples in order to enable output power up signal.) 0 = Disable 1 = Enable (DEFAULT)
		CLKPWRUPEN																	Clock Detection Enable Control 0 = Disable 1 = Enable (DEFAULT)
		REG_SRATE																	Audio Sampling Rate (FS) Select 000 = 16 KHz 001 = 32 KHz 010 = 48 KHz (DEFAULT) 011 = 96 KHz 100 = 192 KHz Others = RESERVED The same ratio for 44.1KHz base
		MCLK_RATE																	MCLK Rate Select (User needs to set the correct MCLK rate by setting this register.) 000 = 12 MHz / 11.025 MHz 001 = 12.288 MHz / 11.2896MHz 010 = 19.2 MHz / 17.64 MHz 011 = 24 MHz / 22.05 MHz 100 = 24.576 MHz / 22.5792MHz (DEFAULT) Others = RESERVED
		FS_MCLK_DET																	MCLK/FS Ratio Detection Enable Control 0 = Disable 1 = Enable (DEFAULT)
		FS_BCLK_DET																	BCLK/FS Ratio Detection Enable Control 0 = Disable 1 = Enable (DEFAULT)
		ZEROCNT_THD																	The Data Zero Threshold Select 00 = 2048 FS (DEFAULT) 01 = 4096 FS 10 = 8192 FS 11 = 16384 FS
		DEFAULT	1	1	0	0	1	0	1	0	0	1	1	0	0	0	0	1	0xCA60 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
41	CLK_CTL2	NOISE_FILTER_THD																	Noise Filter THD Select (Filter out the data noise when the external host is configured mute.) (Step size is -6dB.) 0000 = -72dB 0001 = -78dB ▼ 1011 = -138dB 1100 = -144 dB (DEFAULT) 1100 ~ 1111 = -144 dB
		SEL_BLOCK_SIZE																	DSP Audio Block Size Select 000 = 32 (DEFAULT) 001 = 1 010 = 2 011 = 4 100 = 8 101 = 16 110 = 32 111 = 32
		ANA_SYS_CLK_DETB																	The Analog System Clock Detection Status (RO) 0 = Normal 1 = Abnormal
		AUDIO_CLK_DETB																	The Digital System Audio Clock Detection Status (RO) 0 = Normal 1 = Abnormal
		EN_ABCLK_DET																	Analog BCLK Detection Enable Control 0 = Disable (DEFAULT) 1 = Enable
		EN_DBCLK_DET																	Digital BCLK Detection Enable Control 0 = Disable (DEFAULT) 1 = Enable
		EN_AMCLK_DET																	Analog MCLK Detection Enable Control 0 = Disable (DEFAULT) 1 = Enable
		EN_DMCLK_DET																	Digital MCLK Detection Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	1	1	0	0	0	1	0	0	0	0	X	X	0	0	0	0	0xC0X4 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
46	DEVICE ID	DEVICE ID																	I2C Device ID =1A/1B/4A/4B Depends On The GPIO1 and GPIO 2 During Power On. (RO) 00011010 (1A) = GPIO2 Pull down, GPIO1 Pull down 00011011 (1B) = GPIO2 Pull down, GPIO1 Pull up 01001010 (4A) = GPIO2 Pull up, GPIO1 Pull down 01001011 (4B) = GPIO2 Pull up, GPIO1 Pull up
		CHIP ID																	Chip ID (RO)
		DEFAULT	X	X	X	X	X	X	X	X	1	1	1	1	0	1	0	1	0XXXF5 – R

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
5D	DAC_SINC_CFG	DAC_SINC_OSR																	The OSR of DAC SINC Filter Select 00 = 00 (bypass sinc filter) 01 = OSR=128 (DEFAULT) 10 = OSR=200 11 = OSR=250
		IVSENSE_SINC_OSR																	The OSR of IV _{sense} ADC SINC Filter Select 00 = 16 (DEFAULT) 01 = 32 10 = 64 11 = 25
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x0010 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
5F	ANA_TRIM_CFG1	DLDO_TRIM																	Trim Bits Control Of 1.5V LDO Voltage Select 0000 = lowest ▼ 1111 = highest
		FTRIM_2_0																	The Class D PWM Frequency Trim Bits Select 100 = Default Others = RESERVED
		DEFAULT	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0x8400 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
60	RST	PD_POR5																	5V POR Power Down Enable Control 0 = Disable 1 = Enable (DEFAULT)
		EFUSE_CTL																	Efuse Initialization Enable Control (Load trim value from effuse to related registers.) 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x0010 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
67	ALoop_CFG0	SCP_clear_mode																	SCP Clear Mode Select 0 = Manual clear (DEFAULT) 1 = Auto clear
		SCP_Clear																	Write 1 To Clear SCP Status (0x0069[4]) When SCP_Clear_Mode = 0'b (Manual Mode)
		HV_EN																	Enable Of Class D HV Driver Enable Control 0 = Disable (DEFAULT) 1 = Enable
		SST_EN																	Spread Spectrum Enable Control 0 = Disable (DEFAULT) 1 = Enable
		SST																	Saw-Tooth Current Source Select 0 = Weak (DEFAULT) 1 = Strong
		ANA_MUTE																	Analog Mute Select 0 = Normal play 1 = Analog HV mute (DEFAULT)
		MOD_GAIN																	Class D Modulator Analog Gain Select (Step size is 2dB.) 000 = 6dB 001 = 8dB ▼ 011 = 12dB (DEFAULT) ▼ 111 = 20dB
		CM_COMP_EN																	Class D Modulator Common Mode Voltage Compensation to the V _{BAT} Enable Control 0 = Disable (DEFAULT) 1 = Enable
		V_PBTl																	Setting of PBTl Mode Select 0 = Stereo (DEFAULT) 1 = PBTl mono
		DEFAULT	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0x0160 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
68	ALoop_CFG1	TRIMSCR																	Trim Short Current Reference Select 00 = Low 01 = Mid-low 10 = Mid-high 11 = High (DEFAULT)
		DTX																	Power Driver Non-Overlap Delay Enable Control 0 = Disable (DEFAULT) 1 = Enable
		SEGL																	Segment Driver Control of L Channel Select 0 = Half driving strength (DEFAULT) 1 = Full driving strength
		SEGR																	Segment Driver Control of R Channel Select 0 = Half Driving strength 1 = Full Driving strength (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0x00D4 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
69	ALoop_CFG2	AutoMode_SEGL																	Mapping To 0x0068[4] Automode (RO)
		AutoMode_SEGR																	Mapping To 0x0068[2] Automode (RO)
		Ana_status_OTP																	Analog Status of Over Temperature Protection (RO) 0 = Normal 1 = Abnormal
		Ana_status_OVLO																	Analog Status of Over Voltage Protection (RO) 0 = Normal 1 = Abnormal
		Ana_status_UVLO																	Analog Status of Under Voltage Protection (RO) 0 = Over UVLO voltage Threshold 1 = Under UVLO voltage Threshold
		Ana_status_SCP																	Analog Status of Short Circuit Protection (RO) 0 = Normal 1 = Abnormal
		Ana_status_EN_V2I																	Analog Status of AVDD Ready Status (RO) 0 = AVDD is off 1 = AVDD is Ready
		Ana_status_FAULT																	Analog Status of FAULT Pin (RO) 0 = Normal 1 = Protection triggered
		Ana_status_DC_DET																	Analog Status of DC Detect (RO) 0 = detect w/o DC in the output path 1 = detect w/ DC in the output path
		Ana_status_EN_ALL																	Analog Status of Flag for The Analog Path (Saw-Tooth, MOD, Protection) (RO) 0 = Not ready 1 = Ready
		DEFAULT	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	0x0XXX – R

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6A	SARADC_CFG0	SARADC_EN																	SAR_ADC Enable Control 0 = Disable (DEFAULT) 1 = Enable
		RESETB_SARADC																	Reset of SAR_ADC Select 0 = Reset ADC 1 = Normal (DEFAULT)
		SARADC_CAL																	Auto-Calibration Enable Control 0 = Disable (DEFAULT) 1 = Enable
		SARADC_DIV																	SARADC CLK Divider Select 0 = CLK_ADC => CLK 1 = CLK_ADC => CLK/2 (DEFAULT)
		TRIMSMPL																	Trim Sample Time (48Mhz CLK) Select 000 = 20.83ns (for test mode) 001 = 666.667ns (DEFAULT) 010 = 1.333us ▼ 111 = 4.667us
		VBAT_AVG_EN																	Extra Average Filter Of SAR_ADC V _{BAT} Output for Better SNR And Lower Speed Enable Control 0 = Disable (DEFAULT) 1 = Enable
		VTEMP_AVG_EN																	Extra Average Filter of SAR_ADC Temperature Sensor Output for Better SNR and Lower Speed Enable Control 0 = Disable 1 = Enable (DEFAULT)
		DEFAULT	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0	1	0x5C09 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6B	SARADC_CFG1	VTEMP_EN																	Temperature Sensor Enable Control 0 = Disable (DEFAULT) 1 = Enable
		VBATDIV_EN																	V _{BAT} Divider Enable Control 0 = Disable (DEFAULT) 1 = Enable
		SARADC_VREF_EN																	SARADC VREF Enable Bit Enable Control 0 = Disable (DEFAULT) 1 = Enable VREF Note: Bandgap must be turned on before enable SARADC VREF
		PRELOAD_VREF_EN																	SARADC VREF Pre-Load Enable Control 0 = Disable (DEFAULT) 1 = Enable
		VTEMP_AVG_N																	Strength Of VTEMP Average Filter Select 00 = No average 01 = Average 32 data 10 = Average 128 data (DEFAULT) 11 = Average 512 data
		VBAT_AVG_N																	Strength Of V _{BAT} Average Filter Select 00 = No average (DEFAULT) 01 = Average 32 data 10 = Average 128 data 11 = Average 512 data
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0x0008 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6C	IVSNS_C FG0	PD_VSNS_R																	Right Channel V_{Sense} Disable Control 0 = Enable 1 = Disable (DEFAULT)
		PD_VSNS_L																	Left Channel V_{Sense} Disable Control 0 = Enable 1 = Disable (DEFAULT)
		PD_ISNS_R																	R Channel I_{Sense} Disable Control 0 = Enable 1 = Disable (DEFAULT)
		PD_ISNS_L																	L Channel I_{Sense} Disable Control 0 = Enable 1 = Disable (DEFAULT)
		RESET_SC_VADC_R																	Reset Integration Capacitor of R Channel V_{Sense} Sdm ADC Select 0 = Default (DEFAULT) 1 = Reset
		RESET_SC_VADC_L																	Reset Integration Capacitor of L Channel V_{Sense} Sdm ADC Select 0 = Default (DEFAULT) 1 = Reset
		RESET_SC_IADC_R																	Reset Integration Capacitor of R Channel I_{Sense} Sdm ADC Select 0 = Default (DEFAULT) 1 = Reset
		RESET_SC_IADC_L																	Reset Integration Capacitor of L Channel I_{Sense} Sdm ADC Select 0 = Default (DEFAULT) 1 = Reset
		PBTL_ISEN_E_LR																	Setting Of PBTL Mode Current Sense to DSP Select 0 = Output I _{Sense} (2*R) (DEFAULT) 1 = Output I _{Sense} (L+R)
		PD_LDO_SDM_IVSNS																	Power Down of IV_{Sense} Internal LDO Select 0 = Enable the LDO 1 = Power down the LDO (DEFAULT)
		DEFAULT	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0xF040 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6D	IVSNS_CFG1	PD_V2L_IVSNS																	Power Down of Bias Current Generation for IV_{Sense} Enable Control 0 = Enable 1 = Disable (DEFAULT)
		PD_VREF_SDM_IVSNS																	Power Down of The Reference Voltage for IV_{Sense} Enable Control 0 = Enable 1 = Disable (DEFAULT)
		VSNS_PGA_CUR_SET																	PGA of V_{Sense} Current Select 00 = Small 01 = Middle (DEFAULT) 10 = Default 11 = Large
		VSNS_GAIN_SET																	V_{Sense} Gain Select 00 = 1/24 Gain 01 = 1/20 Gain (DEFAULT) 10 = 1/16 Gain 11 = 1/12 Gain
		VREF_CUR_SET																	IV_{Sense} VREF Buffer Current Select 00 = Small 01 = Middle (DEFAULT) 10 = Default 11 = Large
		ISNS_PGA_CUR_SET																	PGA of I_{Sense} Current Select 00 = Small 01 = Middle (DEFAULT) 10 = Default 11 = Large
		ISNS_GAIN_SET																	I_{Sense} Gain Setting Select 00 = x4 (+12dB) 01 = x8 (+18dB) (DEFAULT) 10 = x12 (+21dB) 11 = x16 (+24dB)
		DEFAULT	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0x3555 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6E	DAC_CFG0	PD_DACL																	L Channel DAC Disable Control 0 = Enable 1 = Disable (DEFAULT)
		PD_DACR																	R Channel DAC Disable Control 0 = Enable 1 = Disable (DEFAULT)
		PD_CHOP_DAC																	DAC Chopper Disable Control 0 = Enable 1 = Disable (DEFAULT)
		DAC_CUR_SET																	DAC Current Cell Current Gain Select 0 = Gain +0dB 1 = Gain +3.2dB (DEFAULT)
		DEFAULT	0	0	0	0	1	1	1	0	1	1	0	1	0	1	0	1	0x0ED5 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
71	CLK_DIV_CFG	IVSNS_CLK_INV_SEL																	IV_{sense} Clock Inverter Select 0 = Normal (DEFAULT) 1 = Inverter
		PD_ANA_CLK																	Power Down of Analog Clock for DAC and IV_{sense} ADC Enable Control 0 = Enable 1 = Disable (DEFAULT)
		CLK_ANA_SEL																	Analog Clock Source Select 00 = MCLK (DEFAULT) 01 = BCLK Others = PLL
		IVSNS_CLK_DIV																	IV_{sense} 16bits ADC Clock Divider Select 000 = Div 1 001 = Div 2 (DEFAULT) 010 = Div 4 011 = Div 5 100 = Div 8 101 = Div 10
		DAC_CLK_DIV																	DAC Clock Divider Select 00 = Div 1 (DEFAULT) 01 = Div 2 10 = Div 4 11 = Div 8
		DAC_CHOP_CLK_DIV																	DAC Chopper Clock Select 0 = 1/16 DAC clock 1 = 1/32 DAC clock (DEFAULT)
		DEFAULT	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0x0211 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
72	PLL_CFG0	PLL_DIV_RESET																	Reset Of PLL Dividers Select 0 = Reset 1 = Not reset (DEFAULT)
		PLLOUT_DIV																	Analog Clock PLL Output Divider Select This register is used when analog DAC/ADC use the PLL divided clock Output divider number = PLLOUT_DIV+1 Ex: 00000 = Div 1 (bypass) ▼ 10011 = Div 20 (DEFAULT) ▼ 11111 = Div 32
		PLL_CLK_SEL																	The PLL Reference Clock Input Select 00 = MCLK (DEFAULT) 01 = BCLK 10 = RESERVED 11 = HIRC48M
		PD_PLL																	PLL Power Down Enable Control 0 = Enable 1 = Disable (DEFAULT)
		PLL_ICP_AUTO_EN																	PLL Charge Pump Auto Current Enable Control 0 = Disabled (manual mode to set ICP current) 1 = Enabled (DEFAULT)
		PLL_ICP_SET																	ICP Current Manual Mode Select 00 = 2.5uA (DEFAULT) 01 = 5.0uA 10 = 7.5uA 11 = 10.0uA
		PLL_KVCO_SET																	PLL KVCO Slope Select 00 = Slope small 01 = Default (DEFAULT) 10 = Slope middle 11 = Slope large
		PLL_BYPASS_LPF_R3																	PLL Loop Filter R3 Bypass Select 0 = Not bypass (R3 filter) 1 = Bypass R3 filter (DEFAULT)
		DEFAULT	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0xCCC4 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
73	PLL_CFG1	PLL_RSEL																	PLL Output Divider Select The divider set the PLL VCO output setting 00 = FVCO div 1 01 = FVCO div 2 (DEFAULT) 10 = FVCO div 3 11 = FVCO div 4
		PLL_MSEL																	PLL Input Divider Select Number = MSEL+1 00000 = Div 1 (bypass) 00001 = Div 2 (DEFAULT) ▼ 11111 = Div 32
		PLL_NSEL																	PLL Feedback Divider Select Feedback Divider Number = (NSEL.XSEL) + 1
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0x0101 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
74	PLL_CFG	PLL_XSEL																	PLL Feedback Divider Select Feedback Divider Number = (NSEL.XSEL) + 1
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
77	SOFT_SD	SW_SD																	Software Shunt Down Mode of Class D Driver Write 0x55AA to shut down (Read:0xFFFF) Write others to enable (Read:0x0000) Before SOFT_SD was set high, user needs to turn off DAC, IV _{Sense} , and SAR-ADC first.
		DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
78	PD_SW_DLDO	PD_SW_DLDO																	Software Power Down Of 1.5V DLDO Write 0xAA55 to disable LDO (Read:0xFFFF) Write others to enable LDO (Read:0x0000) Before turning on DSP and PLL, the internal big LDO must be enabled.
		DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
79	EN_HIRC48M	EN_OSC48M																	Enable OSC48M Oscillator Write 0x5A5A to disable (Read:0x0000) Write others to enable (Read:0xFFFF)
		DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0xFFFF – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
7A	DAC_TRIM_CFG2	DAC_TRIM_TEMP_SLOPE																DAC Channel Temperature Trim Code	
		SARAD_TRIM_RT_OFFSET																SAR ADC Temperature Offset Trim Code at Room Temperature	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W	

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
7B	IVSNS_TRIM_CFG	ISNS_TRIM_TEMP_SLOPE																ISense Temperature Trim Code Slope	
		VSNS_TRIM_TEMP_SLOPE																VSense Temperature Trim Code Slope	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W	

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
7C	MISC_TRIM_CFG	DAC_TRIM_OS_SHIFT																Shift Bit Of DAC_TRIM_OS	
		DAC_TRIM_GAIN_SHIFT																Shift Bit Of DAC_TRIM_GAIN	
		DAC_TRIM_TEMP_SHIFT																Shift Bit Of DAC_TRIM_TEMP_SLOPE	
		ISNS_TRIM_TEMP_SHIFT																Shift Bit Of ISNS_TRIM_TEMP_SLOPE	
		VSNS_TRIM_TEMP_SHIFT																Shift Bit Of VSNS_TRIM_TEMP_SLOPE	
		ISNS_TRIM_GAIN_SHIFT																Shift Bit Of ISNS_TRIM_GAIN	
		VSNS_TRIM_GAIN_SHIFT																Shift Bit Of VSNS_TRIM_GAIN	
		DEFAULT	0	1	1	1	0	0	1	1	1	1	0	1	0	1	0	1	0x73D5 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
7E	CLK_GATE ED_EN	CLK_GATE D_EN																Enable Internal Clock (Except I2C Debounce Clock) Write A5A5 to enable (Read:FFFF) Write others to disable (Read:0000)	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W	

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
86	HW3_CTL0	HW3_dram_clear																	HW3 DRAM Clear Select 0 = Normal run (DEFAULT) 1 = Clear dram
		HW3_stall																	HW3 Stall Select 0 = Normal run 1 = Stall HW3 (DEFAULT)
		DEFAULT	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0020 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
88	ALC_CTL6	UVLOP_VBAT_THRES_HOLD																	UVLOP Threshold Voltage Dec2Hex [Round(123.53 * UVLOP_VBAT_THRESHOLD - 11.08)]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8A	HW3_CTL7	HW3_VOL_VL																	HW3 V _{Sense} Gain Left Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8B	HW3_CTL8	HW3_VOL_VR																	HW3 V _{Sense} Gain Right Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8C	HW3_CTL6	HW3_EN																	HW3 Function Enable Control 0 =Disable (DEFAULT) 1 =Enable
		HW3_DROOP_SEL																	HW3 Droop Mode Select 0 = Large (DEFAULT) 1 = Small
		HW3_FS																	HW3 Input Data Sample Rate Select 0 = 96KHz FS to 48KHz (DEFAULT) 1 = 192KHz FS to 48KHz The same ratio for 44.1KHz base
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8D	HW3_CTL7	HW3_VOL_I L																	HW3 I _{Sense} Gain Left Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8E	HW3_CTL8	HW3_VOL_I R																	HW3 I _{Sense} Gain Right Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8F	HW3_CTL9	HW3_VSR																	HW3 Gain Adjust Slew Rate Select 00 = 0.5 dB (DEFAULT) 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB
		HW3_CH_MUTE																	HW3 Soft Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HW3_Zero_THD																	Zero Sample Threshold of HW3 Set to 0xFF in normal mode
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
90	HW2_CTL0	HW2_dram_clear																	Write 1 Then Write 0 To Clear
		HW2_STALL																	HW2 Stall Select 0 = Normal run 1 = Stall HW2 (DEFAULT)
		DEFAULT	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0020 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
96	HW2_CTL2	HW1_ANC_EN																	3 Band PEQ For HW1 ANC Path Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HW2_EN																	HW2 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HW2_DROOP_SEL																	Droop Mode Select 0 = Small (DEFAULT) 1 = Large
		HW2_DROOP_EN																	Droop Function Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ANC_LATENCY																	HW2 ANC Low Latency Mode Select 0 = Normal (DEFAULT) 1 = Low latency (for ANC path)
		HW2_FS																	HW2 Output FS Select 0 = 96KHz (DEFAULT) 1 = 192KHz The same ratio for 44.1KHz base
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
97	HW2_CTL3	HW2_VOL_L																	HW2 Volume Gain Left Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
98	HW2_CTL4	HW2_VOL_R																	HW2 Volume Gain Right Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
99	HW2_CTL5	HW2_VSR																	HW2 Gain Adjust Slew Rate Select 00 = 0.5dB/step (DEFAULT) 01 = 0.25dB/step 10 = 0.125dB/step 11 = 0.0625dB/step
		HW2_CH_MUTE																	HW2 Soft Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HW2_ZERO_THD																	Zero Sample Threshold of HW2 Set to 0xFF in normal mode
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
9A	HW1_VOL_L_L	HW1_VOL_L																	HW1 Volume Gain Left Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
9B	HW1_VOL_R	HW1_VOL_R																	HW1 Volume Gain Right Channel Register value = Dec2Hex[(-128 - (Target gain (dB))) *128] Register value with 2's complement
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
9C	HW1_CTL_2	MUTE_INTRVL																	Auto_Mute Interval Select The Time Interval Between Digital Mute and Analog Mute When Fault Detected. 00 = 233ms interval 01 = 233ms interval (DEFAULT) 10 = 466ms interval 11 = 699ms interval
		HW1_VSR																	HW1 Gain Adjust Slew Rate Select 00 = 0.5 dB (DEFAULT) 01 = 0.25 dB 10 = 0.125 dB 11 = 0.0625 dB
		HW1_CH_MUTE																	HW1 Soft Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HW1_Zero_THD																	Zero Sample Threshold of HW1 Set to 0xFF in normal mode
		DEFAULT	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0x0800 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
9D	PEQ_CTL	PEQ_BAND																	PEQ Band Numbers Control (Step size is 1band.) 0000 = 1band (DEFAULT) 0001 = 2band ▼ 1111 = 15band
		PEQ_OF-L																	PEQ Left Channel Overflow Flag (RO) 0 = Normal (DEFAULT) 1 = Abnormal(overflow)
		PEQ_OF-R																	PEQ Right Channel Overflow Flag (RO) 0 = Normal (DEFAULT) 1 = Abnormal
		HW1_MEM_WR																	HW1 Memory WriteSelect 0 = Normal run (DEFAULT) 1 = Write coefficient
		HW1_MEM_CLEAR																	HW1 Memory Clear Select 0 = Normal run (DEFAULT) 1 = Clear DRAM
		PEQ_STALL																	PEQ Stall Select 0 = Normal run (DEFAULT) 1 = Stall PEQ(HW1)
		DEFAULT	0	0	0	0	x	x	0	0	0	0	0	0	0	0	0	1	0x0X01 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
A0	LEFT_XO_DRC_CTRL	COEF_RAM_SWITCH_LEFT																	Access XO/DRC Coefficient RAM 1 = Allow I2C R/W XO/DRC Left coefficient RAM 0 = Not allow
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	0x000X – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
A2	RIGHT_XO_DRC_CTRL	COEF_RAM_SWITCH_RIGHT																	Access XO/DRC Coefficient RAM Switch 1 = Allow I2C R/W XO/DRC Right coefficient RAM 0 = Not allow
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	0x000X – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
A4	ANA_REG_0	MSEL_SAW																	PLL_SAW Input Divider Select Input divider number = MSEL+1
		FTRIM_4_3																	The Class D PWM Frequency Trim Bits Selection (Need To Combine With 0x5f[10:8]) FTRIM[4:3] = 2'b10 (default)
		SEL_CLK																	Sawtooth Clock Source Select 0 = Self free run 1 = IV _{Sense} clock
		NSEL_SAW																	Feedback Divider Setting Divider Number=NSEL+1
		DEFAULT	0	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0x7F86 – R/W

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
A5	ANA_REG_1	i_reg_VSAW_LEVEL																	Amplitude Of Sawtooth Select 00 = V _{BAT} < 7V 01 = 7V ≤ V _{BAT} < 13V 10 = 13V ≤ V _{BAT} < 19V (DEFAULT) 11 = 19V ≤ V _{BAT}
		i_reg_KVCO_SAW_SET																	Slope Between PLL Clock & Voltage Select 00 = V _{BAT} < 13V 01 = 13V ≤ V _{BAT} < 19V (DEFAULT) 10 = 19V ≤ V _{BAT} 11 = RESERVED
		RSTN_SAW_PLL																	Reset of Sawtooth PLL APR 0 =Reset
		SHT_IN																	Class D Modulator Input Short Setting for Mute and De-Pop Purpose Select 0 = modulator in normal state 1 = modulator input short for mute and de-pop (DEFAULT)
		HV_EN_SYNC_SAW																	HV_EN Timing Sync to Sawtooth Clock (De-pop) Enable Control 0 = Disable 1 = Enable (Default)
		DEFAULT	0	0	1	0	0	1	1	1	0	1	1	0	1	1	1	0	0x276E – R/W

7 APPLICATION CIRCUIT

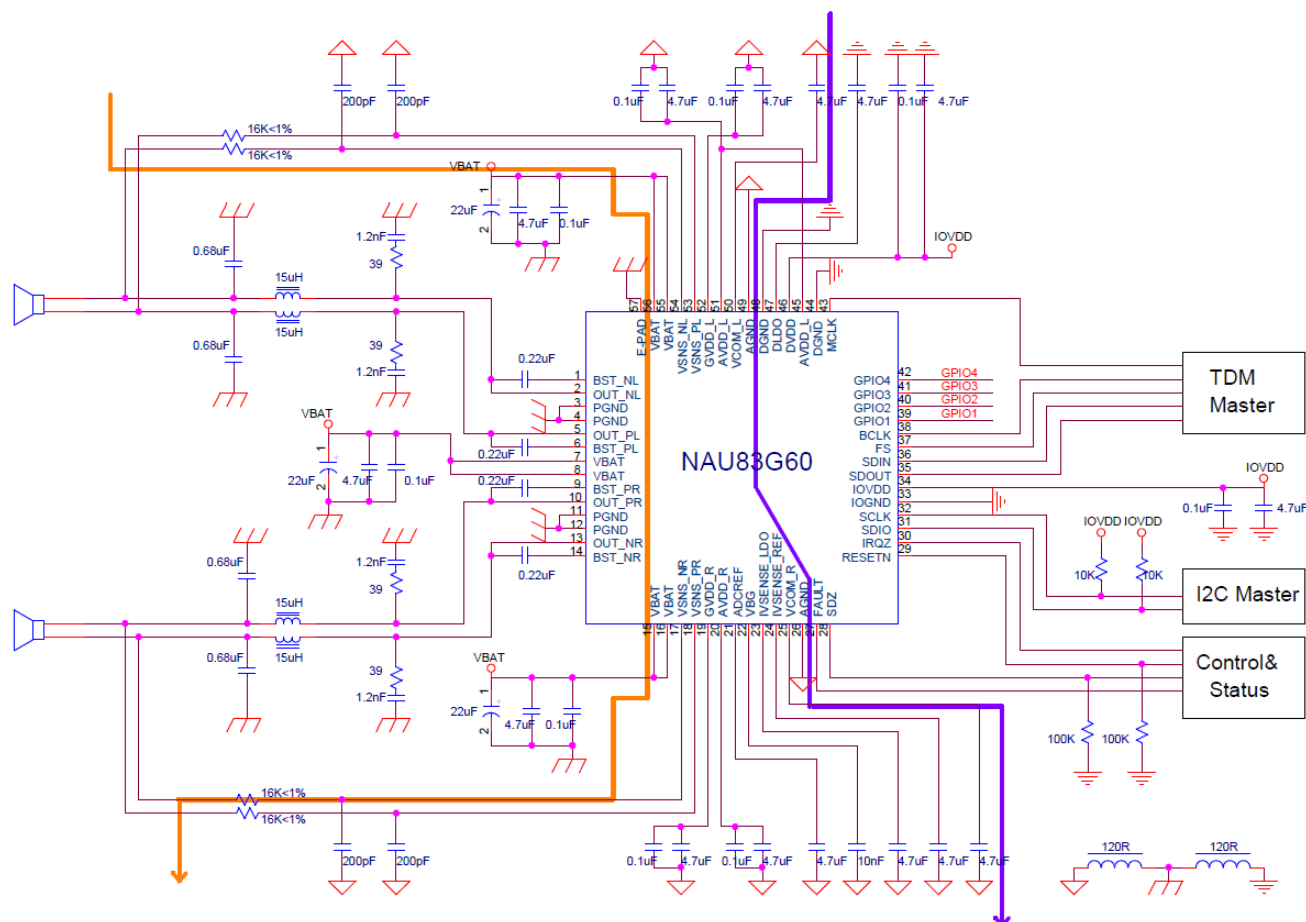


Figure 36 Application Reference Circuit (BTL)

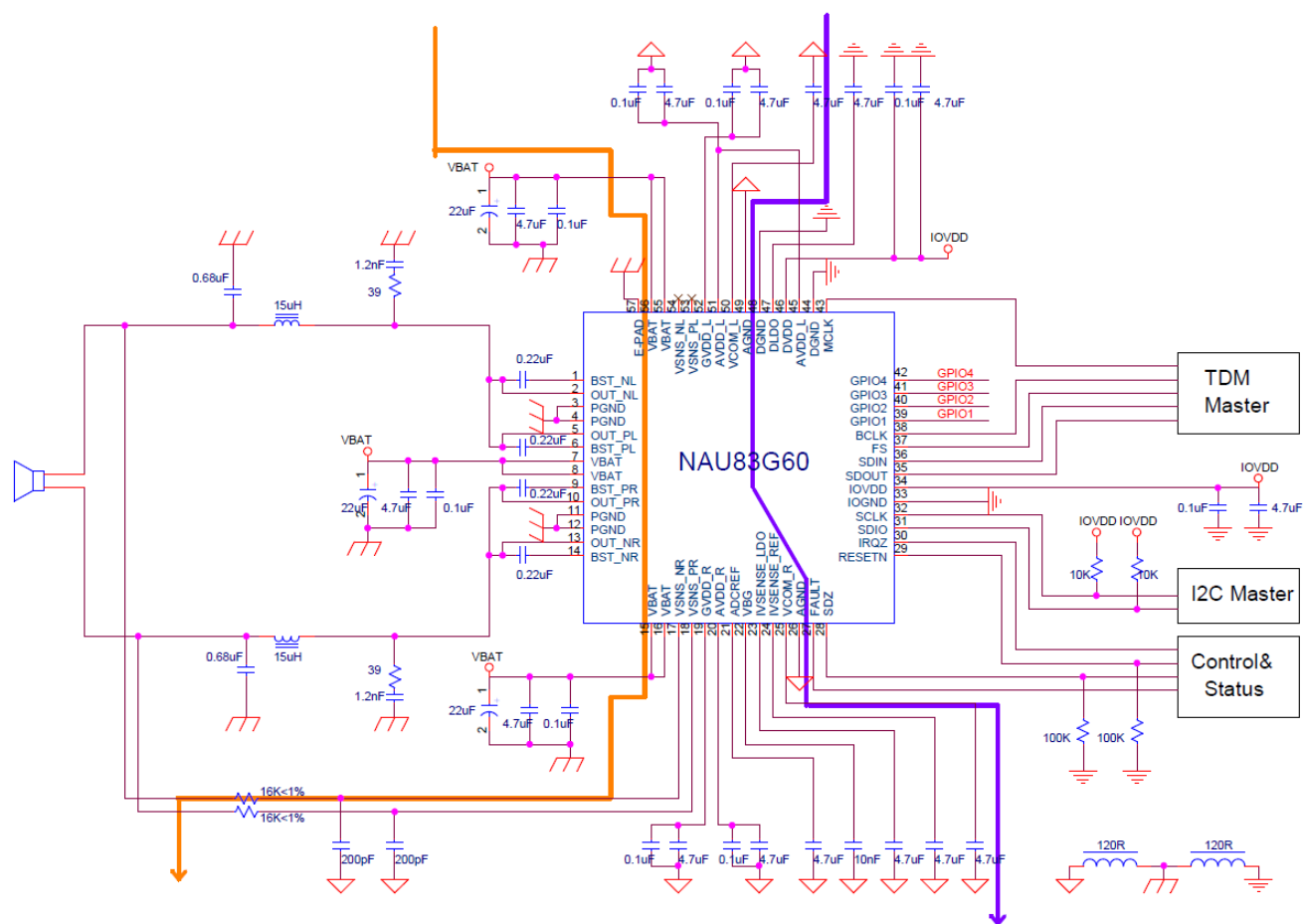


Figure 37 Application Reference Circuit (PBTL)

8 PACKAGE DIMENSION

The NAU83G60 stereo Class-D Amplifier with DSP and IV_{Sense} is available in a small, QFN56 7x7 package, as shown in Figure 38.

QFN 32L 4x4 mm², 0.8 mm thickness (max), 0.4 mm pitch (saw type), EP Size 2.7x2.7mm

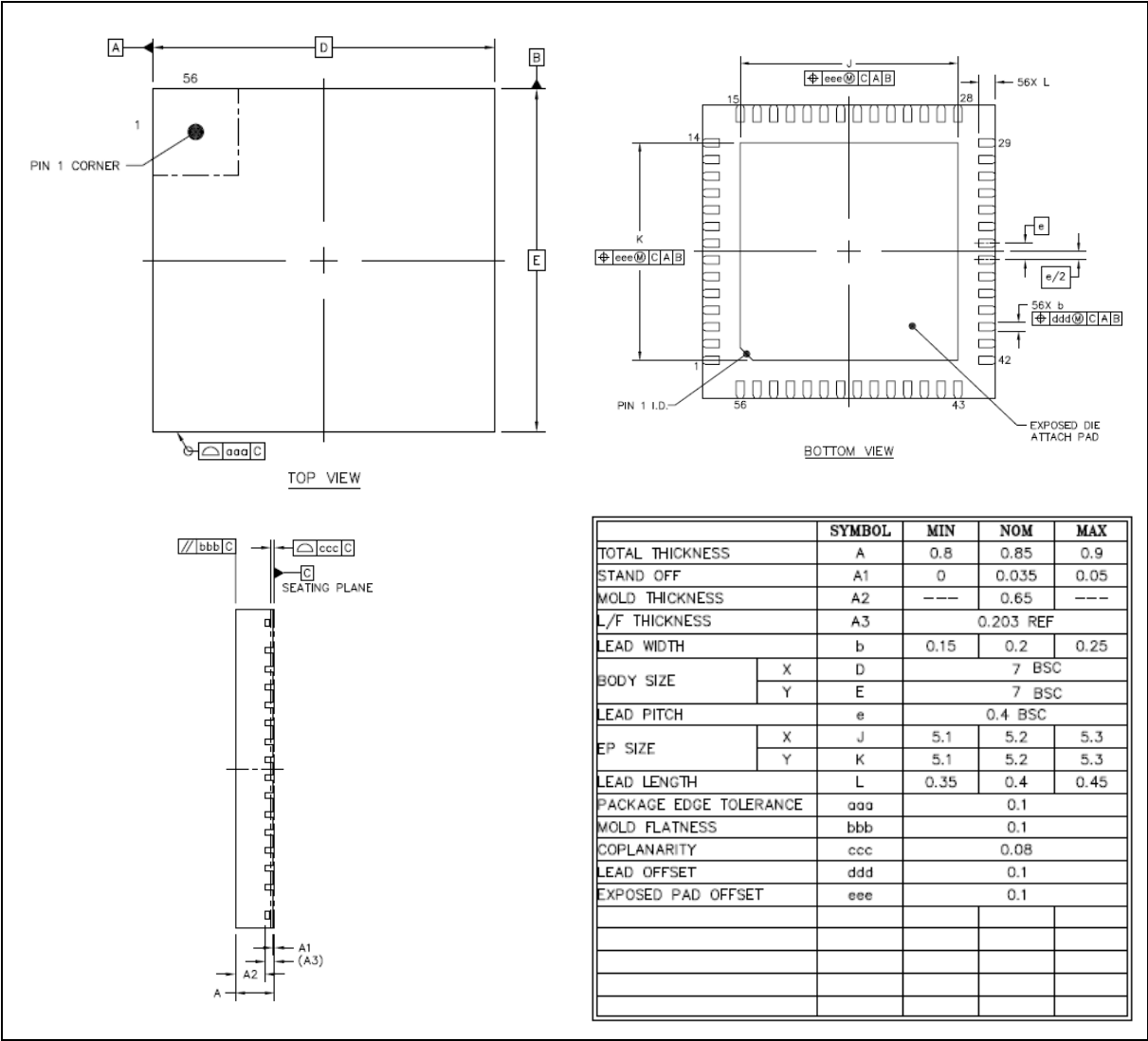


Figure 38 NAU83G60 Package Specification

9 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Jul 2, 2026	Initial Release

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